Multi-Channel Interleaved paralleled phases Shifted Factor Correctors with Passive Control Strategy

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Abstract. High power single-phase PFC such as multi-level interleaved APFC or single-level APFC with multiple power devices in parallel is required for high-power household electrical appliances, communication power and other electric-equipment which are supplied by single-phase AC power source. This paper theorizes an APFC（MxN APFC）with M-channel interleaved N-paralleled switches which is driven by phase-shifted control method. Then the paper analyzes its circuit structure and working principle, including variable ratio of voltage, ripple circuit, driving method and the control scheme. This selection, while maintaining the work frequency of the boost inductor or keeping the same switching frequency of devices, doubles the work frequency of the boost inductor, also, simplifies the inductor design. This paper takes 2x2 APFC as an example of the MATLAB/SIMULINK simulation analysis. The experimental research obtains satisfactory results and verifies that the overall solution is workable.

1.Introduction

The rapid development of power electronic technology has brought great economic benefits and social benefits for the human social production and life. More and more electronic power devices as the intermediate steps of electrical energy transform its access to the single phase or three phase power grid [1], which can improve the electrical energy controllability , but also cause serious harmonic current pollution problems to the grid.

Especially for the power electronic converter which uses diode rectifier bridge and electronic capacitor as the front-end circuit. It produces a large number of harmonic current and reactive power, which greatly reduce the power factor and power utilization, also makes the grid voltage distortion and a huge damage to back-end electric equipment[2].

As the power level of single-phase electrical equipment is increasing everyday, traditional high-power single-stage APFC cannot meet the requirements because of the restriction of power device type selection, high equipment expanse, heat treatment and EMI level. To cater to this trend, multistage interleaved APFC has become the development direction and research focus of high-power APFC[3].

Multistage APFC, used in high power output (greater than 8 kw) equipment, can install boost inductor, but its equivalent ripple frequency equals to the switching frequency of power devices. Also, too large series will cause complex design and control.

This paper, on the basis of the multistage interleaved APFC controlling thought, adopting multiple power devices in parallel, proposes that power devices adopt phase-shifted drive series to improve power level, selection and design of boost inductor and power devices, and carries on theoretical analysis, experimental simulation analysis and implementation study.

2. Circuit Topology

2.1 M-channel Interleaved Single Switch APFC

The circuit of M-channel interleaved APFC, as shown in Figure 1

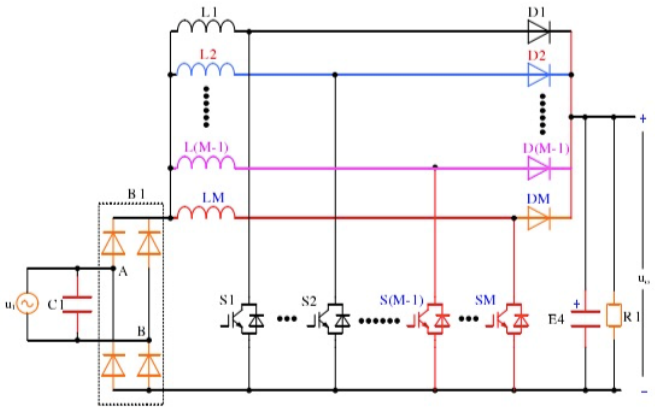

Fig.1 Circuit of M-channel Interleaved APFC

In Figure 1, all levels of APFC share the same voltage output control signal produced by the outer voltage loop. Every level of APFC current inner loop control method of the traditional single-stage APFC, different levels of APFC power device drive pulse overlap each other , or switching period/M. Assuming the carrier frequency is , then the frequency of switching devices in each level of APFC is , the ripple frequency of boost inductor is , the ripple frequency of M-channel inductance synthesis current current is M*.All levels of APFC Share a voltage control loop,the ratio between input and output voltage in each level of APFC is

In the equation, is the output DC voltage, is the absolute value of the input AC voltage, D is the duty ratio of power device, the value of D is in the range of [0, 1],actually the maximum duty ratio can be used is about 0.95.

Because per level of APFC likely works independently, and bears the transmission power Po/M, so the breakover current envelope line and the boost inductor current of the power device are exactly same. The current stress of power device reduces by M times.

2.2 N-paralleled Power Device

(1) Synchronous drive

For single-stage APFC, as shown in Figure 2,when adopting N-paralleled power devices, it is equivalent of one power device if using the same drive signal. Assuming the carrier frequency is , then the switching frequency of power devices is , the ripple frequency of boost inductor is .The voltage ratio between input and output in single-level APFC is same as 4.1.The maximum duty cycle of the power device is close to 1, actually the maximum duty ratio can be used is about 0.95.

Due to the N-paralleled power device, in power device features the same circumstances, each power device transmits Po/N power, therefor the breakover current circuit line of power device is 1/N of the boost inductor current, and the current stress reduces by N times.

If using discrete design, current sharing problem requires special consideration, the greater N is, the more complex the design will be[5].

(2)Phase-shifted drive

For single-stage APFC, as shown in Figure 2, as using N-paralleled power device, if adopting phase-shifted drive signal, it is equivalent of N power devices. Assuming the carrier frequency is , then the switching frequency of power devices will be and the ripple frequency of each boost inductor is N*.

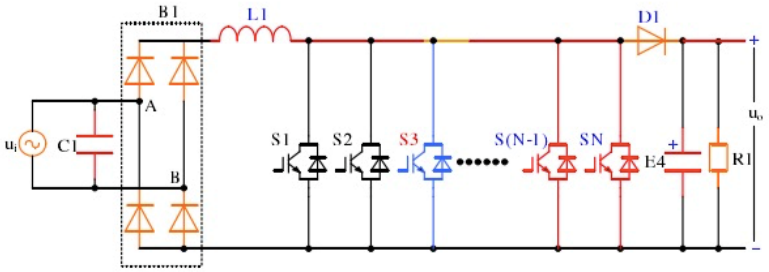

Fig.2 Single-stage APFC with N-paralleled Switches Power Circuit

Single-stage APFC has a voltage control outer loop and a current control inner loop, the only way the final control signal, with two control ways: (1) Use a one-way carrier signal to make the generated original pulse phase-shifted to get N - 1 phase drive pulse;(2) Adopt the phase-shifted N-way carrier signal, respectively, compared with the final control signal to get N-way phase-shifted drive pulse.

For these two cases above, overall the voltage ratio in the single-stage APFC is as same as in the type 1, which means the maximum duty cycle of the power device is close to 1, but because of the stagger conduction, it is easy to deduce that duty cycle of each power device should not be greater than 1 / N, otherwise the sum of duty cycle is greater than 1, which will remain the inductance in state of energy storage and cannot release energy.

In theory, duty cycle of each power device is 1/N of all duty cycle. Its largest duty cycle is close to 1/N, but actually the maximum duty cycle can be used is less than 1/N. Therefor we can obtain that the ripple frequency of boost inductor increases to N times, but the ripple condition is closely related to the waveform change of sine-wave voltage .

Due to the N-paralleled power device, each power device transmits power of Po/N in the circumstances of same power device features. Therefore, the breakover current envelope line of the power device is as same as the boost inductor current. Although the conduction time falls N times, the current stress does not decline.

2.3 M-channel Interleaved N-paralleled Power Device

The power circuit topology of single-phase PFC with M-channel interleaved N-paralleled switch as shown in Figure 3,by inputting single-phase AC voltage will produce DC output voltage and grid side single-phase AC current. Circuit structure mainly includes: diode rectifier bridgeB1 (D1~D4) , boost inductor(L1 ~ LM), reverse fast recovery diode (D1 ~ DM), power devices (S11 ~ S1N,...SM1 ~ SMN), electrolytic capacitor group (E1), filter capacitor (C1) and stable resistance (R1). L1, D1 and S11 ~ S1N constitute the first level APFC, by that analogy, LM, DM and SM1 ~ SMN constitute M-level APFC. N-paralleled switch is included in each level of APFC.

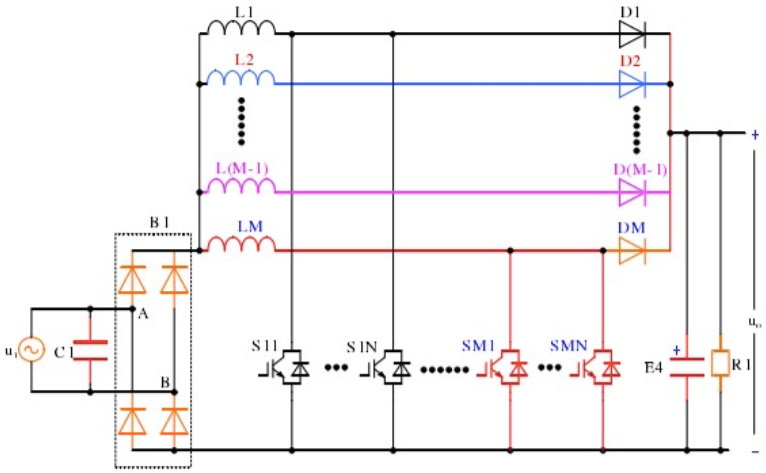

Fig.3 Power Circuit of M-channel Interleaved N-paralleled Swithes APFC

3.Working Principle of MxN-level APFC

As shown in Figure3,in M-channel interleaved N-paralleled power device(phase-shifted) APFC, per-level APFC is responsible for the 1 / M switching period, during each switching period, that level of APFC which belongs to N power device phase-shifted breakover, phase-shifting angle is 360°/MN or switching period/MN. Each APFC is in charge of 1 / MN of the total power. Ripple frequency of inductor is .Ripple frequency of the synthesis total current is .The envelope line of each power device to withstand current is 1 / M of the total inductance current .

According to the analysis, we can set up two kinds of driving modes:

(1) A switching period can be divided into M copies of which every level of APFC possesses. In each copy the N power devices conduct in order, and the phase shifting angle is ,the maximum duty cycle of the power devices is1-1/MN;

(2) Separates a switching period into M copies , N power devices of every level of APFC dispersed into M copies, phase-shifted angle is , the maximum duty cycle of the power device is 1-1/ M.

Taking two-stage double-paralleled switches APFC, for example, as shown in Figure 4, for drive mode 1,during a switching period, the order of breakover of the power devices is S11 - S12 - S21 - S22, the largest duty ratio of the power devices is 0.75.For drive mode 2, during a switching period, the order of breakover of the power devices is S11 - S21 - S12 - S22, the largest duty ratio of the power devices is 0.5.

In consideration of that per level of APFC has a final control signal, there are two kinds of control modes: (1) Use a one-way carrier signal to make original pulse phase-shifted, then get another N - 1 phase drive pulse;(2) Adopt the N-way carrier signal after phase shifting, respectively, compared with the final control signal, then get the N-way phase-shifted drive pulse .

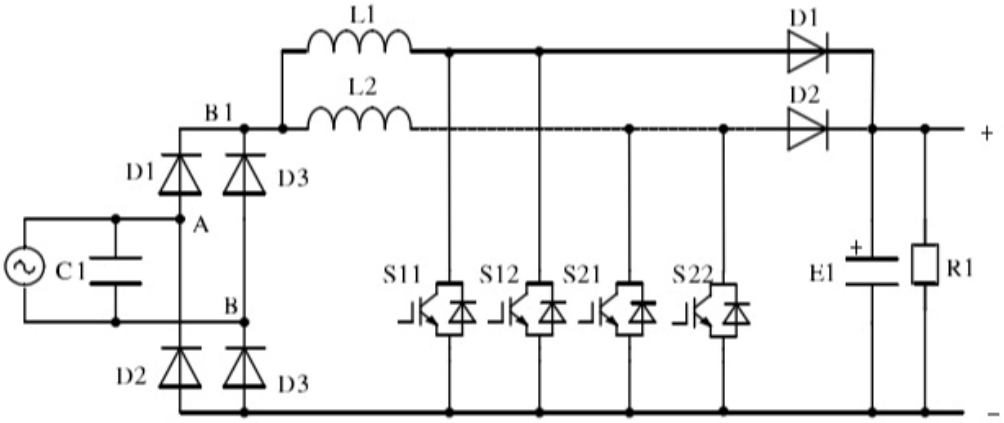

Fig.4 Two-stage Interleaved Twofold Switch in Paralleled APFC Power Circuit

This article adopts the first drive system and the second control mode, for 2 x2 APFC, if four switches devices drive pulse sequences separate from 90 ° , then there are the following switch states:

Duty cycle in (0, 1/4), the quantity of breakover device in chronological order is 1,0,1,0.....;

Duty cycle equals to 1/4, the quantity of breakover device in chronological order is 1,1, 1,1,.....;

Duty cycle in (1/4, 1/2), the quantity of breakover device in chronological order is 2,1, 2,1.....;

Duty cycle is equal to 1/2, the quantity of breakover device in chronological order is 2,2, 1,2,.....;

Duty cycle in (1/2, 3/4), the quantity of breakover device in chronological order is 3,2, 3,2.....;

Duty cycle equal to 3/4, the quantity of breakover device in chronological order is 3,3, 3,3,.....;

Duty cycle in (3/4, 1), the quantity of breakover device in chronological order is 4, 3, 4,3,.....;

When , the circuit topology shows that each inductor has no time to release energy, APFC circuit cannot work normally, which has no practical significance. Sets the duty ratio of a single device to be D, as the output DC voltage, as the input AC voltage, when ,taking L1 branch, for example, as shown in Figure 5.

In the stage of :

In the stage of :

According to the volt-second balance equation:

When ， shown in Figure 6.

At the stage of :

At the stage of :

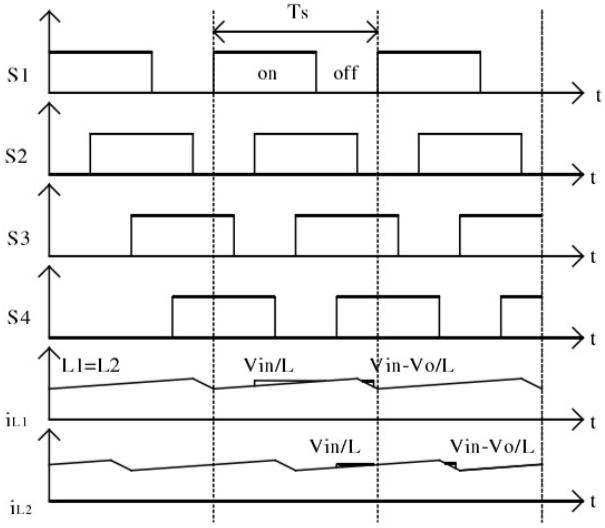

Fig.5 Drive Pulse and Inductance Current Waveform()

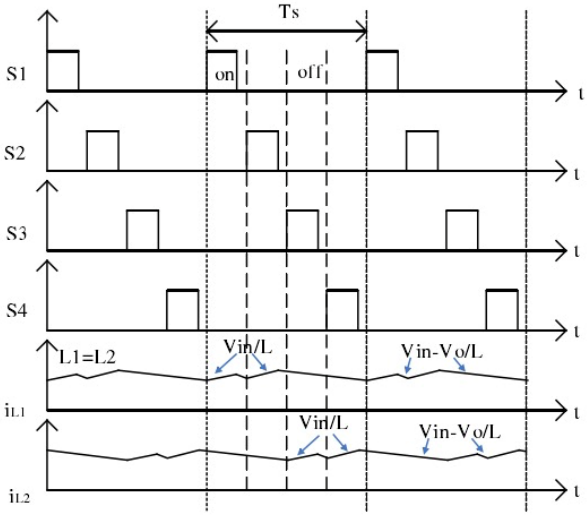

Fig.6 Drive Pulse and Inductance Current Waveform

According to the volt-second balance equation:

On the basis of single-stage APFC device, aiming at the performance index of each boost inductor and power device comparing the characteristics of the above three kinds of control method, as shown in Table 1.

4.Simulated Analysis

Using APFC (2 x2 APFC) with two-level interleaved two-paralleled device phase-shifted driver to carry on a simulation analysis and adopting passive control strategy, a group of trigger rule of one APFC level as shown in Figure 7, the overall 2 x2 APFC power circuit and control circuit as shown in Figure 8.

The simulation parameters are as follows: input is single-phase AC sine voltage 220 v, expected output DC voltage is 385V.System switching frequency is 25kHZ.Boost inductor value L1 and L2 is 1.0mH, its equivalent resistance in series is . Load resistance is 42.35 W, and rated load power is 3.5 kW. The grid side fundamental current effective value is 16.9 A, and the peak value is 22.5 A. Considering the actual data of the power circuit, FRD forward blocking voltage drop is 1.5 V, IGBT forward voltage drop is 1.7 V, this moment conduction equivalent resistance is 0.2Ω and rectifier bridge diode voltage drop is 1.5 V. Ac capacitor C1 is , and ESR is . Electrolytic capacitor group E1 is and the ESR is .

Injecting damping resistance selection , system with the rated load, Figure 9 shows 2 x2 APFC input voltage and input current simulation waveforms, the input current in diagram is standard sine wave , the input power factor is 1.The total harmonic content of input current is 2.13% [4].Due to

the energy control, the response speed of current loop is higher than the traditional control method. Two-level inductor current and synthetic inductance current waveform shown as Figure 10, the current waveform of power devices shown as Figure 11, the output DC voltage waveform shown as Figure 12. The simulation result shows that the passive control can achieve good control effect.

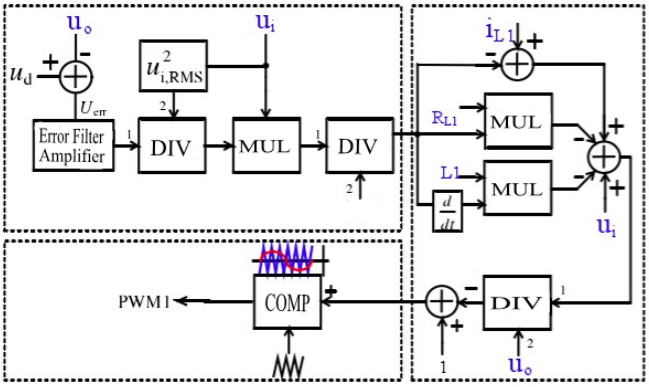

Fig.7 Passive Control System Structure of 2x2 APFC

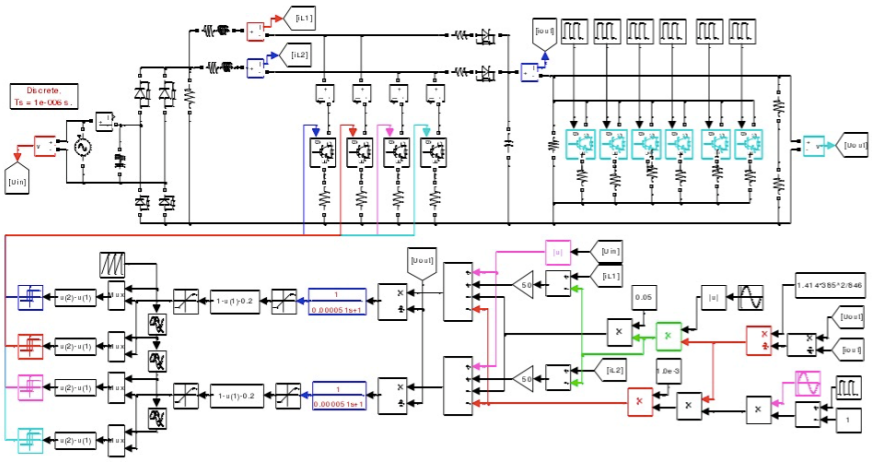

Fig. 8 Passive Control System Simulation Circuit of 2 x2 APFC

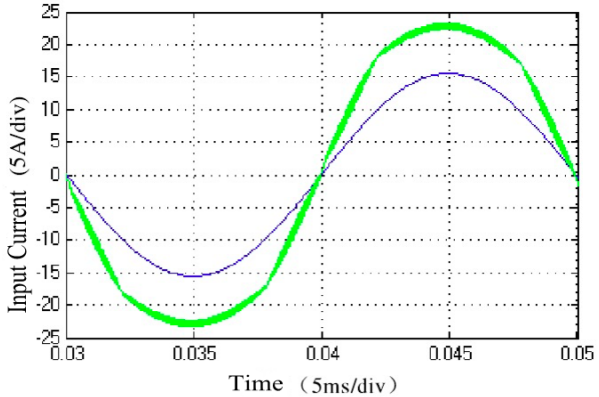

Fig. 9 The Grid Side Input Voltage and Radio Waveform When Rated Load

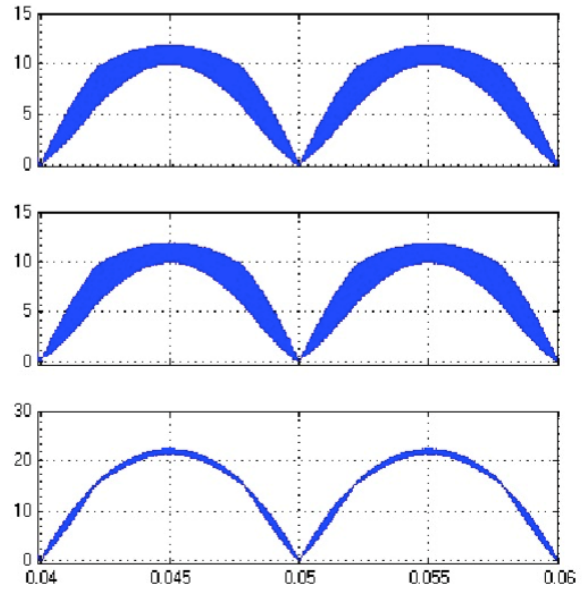

Fig.10 Each Level of Inductance Current and Synthetic Current(at the same inductance value)

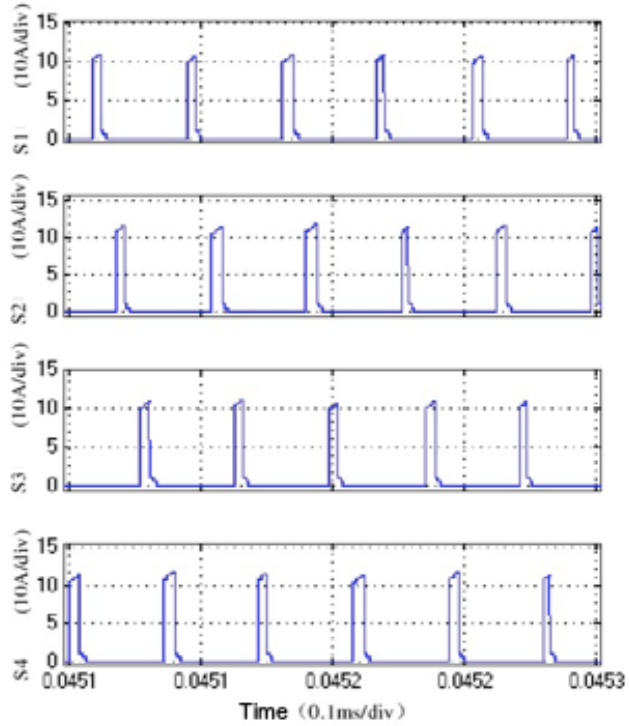

Fig.11 The Current Waveform of Power Devices

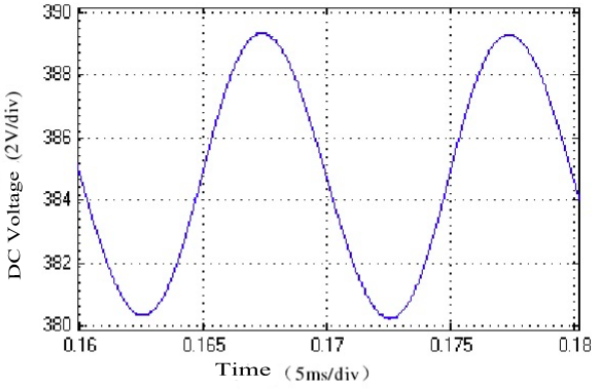

Fig. 12 Output DC Voltage Waveform

5.Conclusion

After describing M-channel interleaved single switch APFC and N-paralleled power device, this paper introduces the control structure and working principle of a new type of APFC with M-channel interleaved N-paralleled phase-shifted power device, including voltage change, drive mode and control mode, which can reduce the switching frequency of power devices and maintain the work frequency of the boost inductor unchangeable, or keep the same switching frequency of power devices to increase the work frequency of boost inductor by times. It meets standards of the high power applications, and also solves the current sharing issue of IGBT paralleled current. Taking 2 x2 APFC as an example, with the passive control strategy, a MATLAB/SIMULINK simulation analysis[6] is carried on to prove that APFC has good static and dynamic characteristics and stronger robustness by parameter perturbation.

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