Research on Real-time Multi-rate Simulation of High Frequency Converter

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Abstract. In order to solve the problem that simulation accuracy and simulation flexibility is difficult to take into account in real-time simulation of high frequency converter, a real-time multi-rate simulation method based on FPGA+PC is proposed. This method fully demonstrated the simulation principle of multi-rate co-simulation system and modeling method, and the process of hardware architecture design implementation. In this paper, a high frequency two level voltage source converter is selected for real-time multi-rate simulation test. Take off-line accurate simulation results as benchmark, we demonstrated comparison of simulation waveform, simulation error and simulation error between multi-rate co-simulation platform and PC real-time simulation platform. The result shows the validity of this multi-rate real-time simulation platform.

Introduction

In recent years, the development of renewable energy such as wind energy, high frequency converter which can reduce the harmonic distortion and the use of power filter, has become the mainstream of the future power grid[1-2]. This makes the power real time simulation for high frequency converter system become more and more important in the development, testing, engineering design and other fields[3]. But the development of the high frequency converter technology has brought the challenge of the power electronic real-time simulation. On the one hand, In the field of automation, industrial electronics, marine, aerospace propulsion, the typical power electronic converter switching frequency is 10-200KHz[3-4]. To guarantee the accuracy of the simulation, the power simulation step is usually required in the power switch cycle of 1/20, requiring nanosecond simulation step[3]. On the other hand, it is also needed to have a flexible modeling capability in real-time simulation of controller. At present, the typical power simulation platform based on multi-PC or multi-DSP can reach only a few microseconds[3,5-6], while FPGA which has high parallel processing capability and the nanosecond range simulation potential are considered as the most promising research directions of power real time simulation[3,7]. The simulation platform based on FPGA and DSP is much less flexible in modeling than PC based simulation platform. In 2004, Pekarek Steven proposed an off-line multi-rate simulation method which combines variable step with fixed step[8]. In 2009, Toshiji Kato proposed the power electronic multi-rate analysis method for circuit partitioning[9]. Roy Crosbie applies real time multi-rate simulation method in ship power[10]. Multi-rate co-simulation based on multi-processor is the development trend of power electronic real time simulation platform.

On the basis of the above research, this paper applies the multi-rate simulation method to the real-time multi-rate co-simulation platform based on FPGA and PC. In the practical high frequency converter system, the frequency response of the controller part is relatively slow (the sampling period is 100us to ms), and the frequency response of the power electronic circuit is faster (10-200kHz)[5]. Therefore, in this paper, the slow response parts such as controller are simulated by PC, and the simulation of power electronic circuit is completed by FPGA.

Platform architecture and design implementation

Multi-rate simulation principle and system design. For the simulation system, the most fundamental problem is how to model and how to use integral solution method. In power system transient simulation modeling, the node analysis method and the state space method are two main directions, and the state space method is widely used in FPGA real-time simulation . In the integral solution, the fixed step integration method has a relatively stable calculation quantity, and can guarantee real-time performance, the vast majority of real-time simulation using the method. The large scale power system including the high frequency converter and other switching devices includes the slow response control part and the fast response circuit. In order to improve the efficiency and flexibility, this paper uses the multi-rate fixed step state space method.

Assuming that the PC simulation step is h_s, FPGA simulation step is h_f. It is required that the low speed simulation step should be an integer multiple of the high speed simulation step. That is:

$$h_s = N \cdot h_f, \quad N \in \mathrm{N} \tag{1}$$

The state space equation of the corresponding multi -rate simulation system can be expressed as:

$$\frac{dX}{dt} = \frac{d}{dt}\begin{bmatrix} X_f \\ X_s \end{bmatrix} = \begin{bmatrix} F_f(X_f, Y_s, t) \\ F_s(X_s, Y_f, t) \end{bmatrix} \tag{2}$$

$$Y_f = G_f\left(X_f\right), Y_s = G_s(X_s) \tag{3}$$

Where X_f and X_s are the state of high-speed and low speed subsystem. Y_f and Y_s are coupling term of high speed and low speed systems. Whatever the integral solution, it can be written as formula (4) (5).

$$\begin{aligned} X_f(t_f^{m+1}) = & \sum_{i=0}^{p-1} \alpha_i X_f\left(t_f^{m-i}\right) + \\ & h_f \sum_{i=-1}^{p-1} \beta_i F_f\left(Xf\left(t_f^{m-i}\right), Y_s\left(t_f^{m-i}\right), t_f^{m-i}\right) \end{aligned} \tag{4}$$

$$\begin{aligned} X_s\left(t_s^{m+1}\right) &= X_s\left(t_s^m\right) + h_s \sum_{i=1}^{r} \alpha_i k_i \\ k_i &= F_s\left(X_s\left(t_s^m\right) + h_s \sum_{j=1}^{p} \lambda_{ij} k_j, \right. \\ & \left. Y_f\left(t_s^m + \mu_i h_s\right), t_s^m + \mu_i h_s\right) \end{aligned} \tag{5}$$

Here h_f and h_s are high-speed and low speed simulation step, t_f^m and $t_s^m (m = 0,1,\cdots)$ are the sampling time of high-speed and low speed subsystem. When the change of X_f is much faster than X_s, it can be set to $h_f = h_s$. By formula (3), we can calculate the amount of the coupling in each subsystem, and bringing into the formula (4) (5) to calculate the update value of the state variables.

However, in the real time simulation of high speed system and low speed system, the sampling rate of the coupling term original data is not consistent with the sampling rate of the state variable to be solved.So it is necessary to convert rate of coupling term.

The paper[13] presents a conversion method of coupling term sample rate between different rate subsystems in multi-rate simulation shown in figure 1. By h_s step sampling and first order, the slow subsystem output Y_f is transformed into U_f ,entering fast subsystem. By the dynamic mean, h_s step sampling and zero order holder,the output Y_s of the fast subsystem is transformed into U_s ,entering slow system. The conversion error E_1 and E_2 are introduced into the process.

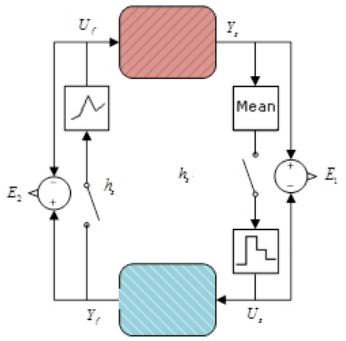

Fig. 1 Diagram of data transmission between subsystems in multi-rate simulation

The paper[13] proved that the conversion error brought by the multi-rate simulation method is convergence and very small when the coupling term amount of interaction between the subsystems is linear, which can meet the demand of the power simulation accuracy.

This pape combines the multi-rate simulation method with real-time high frequency converter system simulation application based on the above simulation theory. The low subsystem is simulated by PC. The fast subsystem of power electronic circuit is simulated by FPGA simulation card. Two subsystems form real-time multi-rate co-simulation. Simulation platform architecture is shown in figure 2. PC uses industrial control computer running QNX real-time operating system. FPGA uses the ML605, 100MHZ simulation system clock frequency.

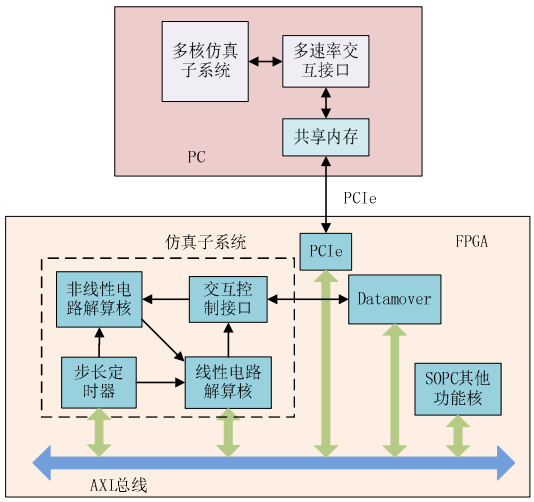

Fig. 2 Architecture of FPGA and PC real-time multi-rate co-simulation platform

Clock synchronization. To carry out FPGA and PC co-simulation, the first premise is that the FPGA simulation and PC simulation process have a unified real-time simulation clock.

This paper takes FPGA as the main control unit of the simulation clock, and FPGA timer generates the corresponding simulation clock to the FPGA solver and PC.

When the counter of the FPGA low speed part's step reach the set value, the PCIe bus through the TLP message to the PC specified memory location to write a time stamp. When the PC detected the time stamp, starting a step simulation calculation. This synchronization method can ensure that the FPGA and PC are only a few hundred ns step trigger error, and this error is relatively stable. The simulation step jitter controlled by this method is small enough to meet the requirements of PC high speed real-time simulation.

Simulation data interaction. The PC and FPGA co-simulation also need to be able to complete the real-time data exchange of multi-rate simulation. According to the second section of the theory, from PC to FPGA, it is from low speed to high speed conversion,by the use of first order hold(linear extrapolation); from FPGA to PC,it is from high speed to low speed conversion, by the use of dynamic mean zero order hold. Data conversion effect is shown in figure 3.

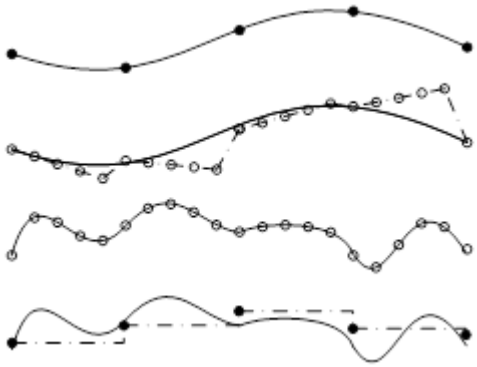

Fig. 3 Diagram of multi-rate simulation data transmission

This part of the data exchange is based on the PCIe bus using high-speed data transmission control IP core (AXI Datamover) to achieve. As shown in Figure 4, when h_s is detected each time, MM2S_CMD commands and S2MM_CMD commands are issued by the data exchange control core to the AXI Datamover control core. The MM2S partial transfer channel obtains coupling data Y_s of the PC simulation sub-model from the PC shared memory area mapping from AXI BAR. The data is passed to the first order holder and is imported into input update register of the FPGA high speed subsystem simulation part. The S2MM transfer channel interface obtains average value of coupling data Y_f from the FPGA simulation sub-model, then writes coupling data to the BAR AXI shared memory area on the PC. The data is passed to zero order hold and then enter low speed simulaton subsystem.

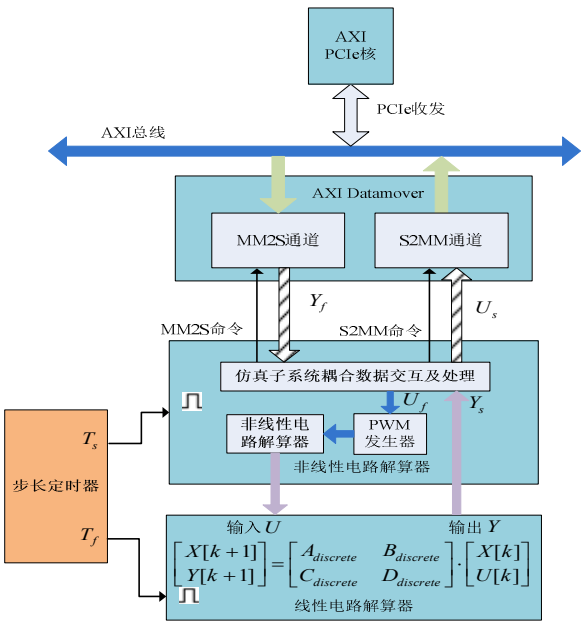

Fig. 4 Diagram of multi-rate simulation data communication

Case simulation experiment and analysis of the results

Take SimPowerSystem simulation model of the three phase two level inverter case as a benchmark, shown in Figure 5. The three phase measuring unit is inserted between the AC side of the inverter bridge and the transformer Y_g terminal to observe the phase voltage and line current. Set SPWM wave carrier frequency 10kHz, the modulation ratio 1. Set simulation step 0.5us. The case is composed of PC control sub-model, FPGA nonlinear sub-model and FPGA linear sub-model in mulit-rate co-simulation platefprm. Invoking the power_analyze function, we can convert the linear circuit model to the state space equation:

$$\begin{bmatrix} \dot{X} \\ Y \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} X \\ U \end{bmatrix} \tag{6}$$

X is the system state, Y is the system output, U is the input of the system. The state space equation is discretized by using the trapezoidal method:

$$\begin{bmatrix} X[k+1] \\ Y[k+1] \end{bmatrix} = \begin{bmatrix} A_{discrete} & B_{discrete} \\ C_{discrete} & D_{discrete} \end{bmatrix} \cdot \begin{bmatrix} X[k] \\ U[k] \end{bmatrix} \tag{7}$$

As shown in Figure 5, the nonlinear solver and the linear solver are parallel computing.The input of nonlinet solver is obtained from the output vector Y of the linear solver, and the output of the nonlinear solver is fed back to the input vector of U the linear solver. In the FPGA simulation board, solving process of linear circuithe linear is matrix multiplication vector operation shown as (7) in each simulation step. PC is used to simulate the control model which generates modulating signal.

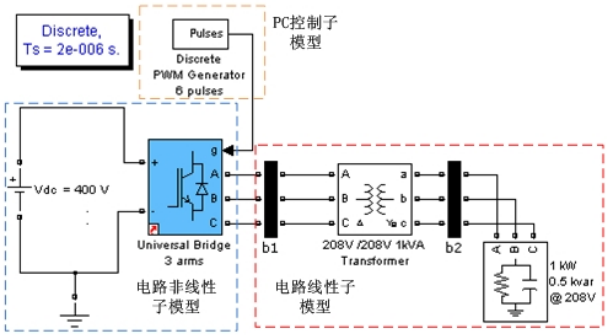

Fig. 5 Diagram of three phase two level inverter case

In the multi-rate co-simulation, the control simulation sub-model adopts 10us simulation step in PC, and the power electronic circuit part (including linear and nonlinear Solver) adopts 0.5us simulation step in ML605 FPGA board.

Multi-rate co-simulation, SimPowerSystems simulation benchmark and PC real-time simulation (10us) are compared with the results of Figure 6, 7. Figure 6 is comparison of simulation results in load's phase AB, Figure 7 is the comparison of simulation results in inverter's phase A current. It can be seen that the multi-rate co-simulation results are consistent with the simulation results, and the PC real-time simulation result is in large errors.

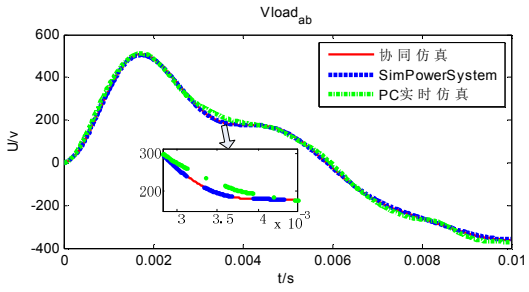

Fig. 6 Comparison of simulation results in load's phase AB voltage

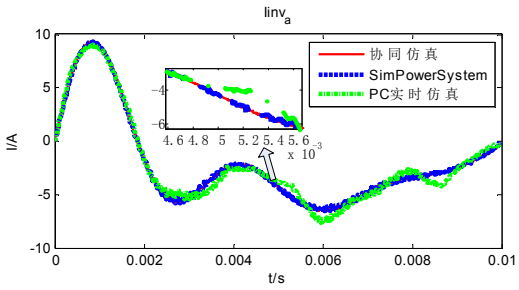

Fig. 7 Comparison of simulation results in inverter's phase A current

Conclusions

The FPGA and PC mulit-rate co-simulation platform designed by this paper can carry out analysis of the high frequency converter system efficiently and in real time.

In the simulation test, it can be seen from the comparison of the simulation waveforms: the simulation accuracy of this platform has a great improvement compared with the PC real-time simulation platform, and the fitting of the electromagnetic transient is more accurate, and the error is about 1%.

This simulation platform has important significance in the power system analysis, especially in the micro grid testing, analysis and other engineering applications.

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