The Design of the DSP Control Circuit in the Conversion Device of Power Source about Medium Frequency Generator

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Abstract: This paper describes the design of control circuit which makes the TMS320LF2407 as the core. It mainly introduces the characteristics of DSP, the general development process of DSP system and the DSP chip TMS320LF2407's characteristics adopted by this system. It focused on the peripheral circuit design of TMS320LF2407, which mainly includes DSP power circuit, DSP clock circuit, RAM interface circuit with the outside extension of DXDSP, JTAG simulation interface circuit of DSP, reset circuit of DSP, etc. In order to realize the strategy of the DC bus voltage feed forward control, and adopt the DSP chip TMS320LF2407 with high-speed processing capability as the control chip, we design the control circuit of the whole system. This paper mainly describes the characteristics of TMS320LF2407 and the design of control circuit which makes the TMS320LF2407 as the core.

Introduction

With the development and the improvement of control strategies and control implementation means, especially the rapid development of digital signal processing technology, digital control technology of power electronics has a broad development space. Practice has proven that adopting digital control technology is not only the inevitable means to realize the modularization, integration and miniaturization but also has the advantages of precise control, reliable and stable work, low loss, high efficiency, etc at the same time. Therefore, now it is the mainstream direction with the development of the power electronics.

The advantages of DSP system can be seen as follows.

1) The interface is convenient. DSP system and other systems or devices based on modern digital technology are mutually compatible.

2) The programming is convenient. Programmable DSP chip can make the design personnel modify and upgrade the software flexibly and conveniently in the process of development.

3) It has good stability. Based on digital processing DSP system has high reliability and is less affected by environment, temperature and noise.

4) It has high precision. A simple 16 digit system can achieve the accuracy of 10-5.

5) It has good repeatability. The performance of the simulation system is affected by the change of Component parameters performance largely. While the digital system is basically not affected. Therefore, the digital system is easy to test, debug and have mass production.

6) The integration is convenient. The digital components in DSP system have a high degree of standardization to facilitate large-scale integration.

The General Process of DSP System Development

The general process of DSP system development can be seen as follows.

1) We should determine the system requirements of the performance index and signal processing.

2) We should get the algorithm simulation according to the system requirements. Generally speaking, in order to achieve the ultimate goal of system, the input signal needs to be properly dealt with. While the different processing methods will lead to different performance of the system. If we

want to get the best system performance, we must determine the best treatment method in this step, namely the digital signal processing algorithms.

3) We should design DSP system. The design of DSP system includes two aspects, namely hardware design and software design. For hardware design we should first choose the right DSP chip according to the computation of the system, operational precision, syste's costs, volume, power consumption and other requirements. Then we should design the peripheral circuit and other circuits of DSP chip. For software design we should write the corresponding DSP assembler mainly based on the system requirements and the selected DSP chip. If there is the support of high-level language compiler, the high-level language (such as C programming language) programming can be used too.

4) We should debug hardware and software. Usually we debug software by the aid of DSP development tools, such as software simulator, DSP development system or emulators, etc. After the debugging with hardware and software of the system are respectively completed, we can make the software be separated from the development system and be run directly on the application system. Of course, the development of DSP system, especially the software development, is a process which requires repeated. If the algorithm computation amount are too large to be run on the hardware in real time, we must modify or simplify the algorithm.

The Introduction of TMS320LF2407A

TMS320LF2407A is a fixed-point DSP chip from the C2000 series of TI company, and its every performance has been improved to a large extent. It provides the practical applications with the solution of low cost, low power consumption, and high computing power. It is very useful for the digital control of motors, inverters and other things. Advanced peripherals are integrated into the chip to form a true single chip controller.

Generally speaking, TMS320LF2407DSP has the following features.

1) We should adopt static CMOS technology with high performance to make the voltage of the power supply drop to 3.3V and reduce the power consumption of controller. 40 MIPS execution speed makes the instruction cycle be shortened to 25 ns (40 MHZ) so as to improve the real-time control of the controller.

2) CPU core based on the TMS320C2xxDSP makes sure of DSP code compatibility between TMS320LF240xseries and TMS320C2xx series.

3) There are FLASH program memory with the storage space of up to 32K bytes, data /program RAM with the storage space of up to 2.5K bytes, dual-port RAM (DARAM）with the storage space of up to 55K bytes, and single-port RAM (SRAM）with the storage space of up to 2K bytes on chip.

4) The two event manager modules, namely EVA and EVB. Each module contains two 16 bit universal periodic interrupt timers and eight 16 bit pulse width modulation (PWM) channels. They can achieve the following things, such as the three-phase inverter control; symmetric and asymmetric waveform of PWM; When power protect is interrupted the pin $\overline{PDPINT}$ will shut PWM channels fast with low electricity at ordinary times; The dead zone control of Programmable PWM can prevent the upper and lower bridge arm from outputting trigger pulse at the same time; three capture units; interface circuit of optical encoder on chip; A/D converter with 16 channels. The module of event manager is suitable for AC induction motor, brushless DC motor, switched reluctance motor, stepper motor, multistage motor and inverter, etc.

5) It can extend external memory with the storage space of 192K bites, program memory with the storage space of64K bites, data memory with the storage space of 64K bites, and I/O address space with the storage space of 64K bites.

6) Watchdog timer module(WDT）.

7) The minimum conversion time of 10 bit A/D converter is 500ns. We can choose the two event managers to trigge two input A/D converters with 8 channels or an input A/D converter with 16 channels

8) 2.0 B module of controller area network（CAN）

9) Serial communication interface（SCI）

10) 16 bits serial peripheral interface module（SPI）.

11) The clock generator Based on the phase-locked loop.

12) Up to 40 general input/output pins which can be programmed individually and reused（GPIO）.

13) Five external interrupts(Motor drive protection, restoration and two maskable interrupts)

14) Power management consists of 3 low power consumption modes. And it can independently turn peripheral device into low power consumption mode.

The Peripheral Circuit Design of TMS320LF2407A

Because PWM module, AD conversion module and other necessary peripherals of digital control are integrated in TMS320LF2407A, the design of the peripheral circuit is greatly simplified.

DSP Power Supply Circuit. Because the working voltage of DSP is +3.3V instead of +5V which is used by microcontroller usually, we need to add a voltage conversion module RC1117 to make the + 5 v output voltage of auxiliary power circuit be converted into the + 3.3 v voltage which is required by DSP's work. In addition, in order to guarantee the sampling precision of AD converter module and improve the anti-interference ability, we need to adopt the inductors L1 and L2 as shown in Figure 1 and the capacitor C20 to make analog supply voltage AP3P3and digital power supply voltage P3P3 of AD conversion module be seperated with ADC analog ground AGND and digital ground DGND.

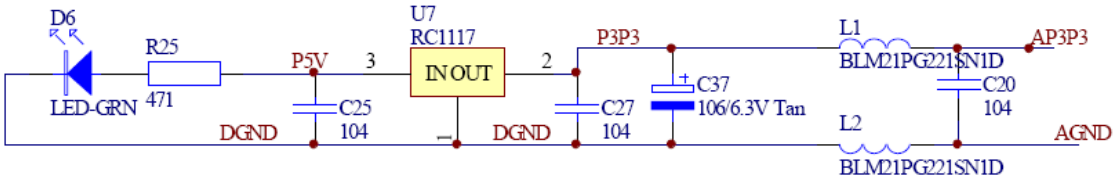

Figure 1 DSP Power Supply Circuit

DSP Clock Circuit. Clock circuit is used to provide the system clock to DSP chip. Generally speaking, there are two ways to provide the system clock. One way is to make the external clock source directly be input XTAL1 / CLKIN pin and make XTAL2 be hung up. The other way is to make use of the crystal circuit which is supplied by the inside of DSP chip to connect an internal oscillator with passive crystal which can be started between XTAL1/CLKIN and XTAL2 on the DSP chip. This system adopts this method and uses crystal oscillator with 10 MHZ, as shown in Figure 2 (a).

TMS320LF2407 has phase-locked loop circuit with internal locks. It can pass frequency doubling circuit with phase-locked loop from a lower external clock to realize the internal frequency doubling. It is very useful for the electromagnetic compatibility of the whole circuit board because the outside only requires crystal oscillator with the lower frequency to avoid external circuit interfering with the clock. At the same time it can also avoid the high-frequency clock interfering with other circuits on the board. PLL module of TMS320LF2407 uses external filter to suppress the signal jitter and electromagnetic interference so that it can minimize the signal jitter and disturbing influence. The external filter circuit of this system is composed of the capacitors, namely C3, C4 and R9, as shown in Figure 3 (b). Filter circuit loop is connected to DSP chip's PLL1 pin and PLL2 pin. We must pay special attention to traces which is connected with PLL should be as short as possible [15].

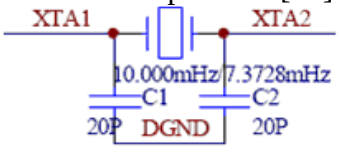

Figure 2 (a) DSP Clock Circuit

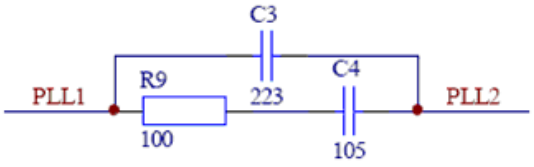

Figure 2 (b) DSP Clock Circuit

RAM Interface Circuit with DSP External Expansion. Although the inside pf TMS320LF2407A has had nearly 4K RAM, it still can't meet the system's needs of complex operation. Especially at the debugging stage of system software, it needs to debug the program in external RAM. Therefore, it generally needs to carry on RAM's external expansion. Because the structure of DSP, the working way is different from the general single-chip microprocessor, there are some special requirements for the external storage. The most critical problem of them is the speed matching problem between the storage and DSP. There are two kinds of working ways for the external memory of DSP system. One working way is zero waiting, and the other working way is inserting waiting period. When read-write speed of the external memory is fast enough and data release time is short enough, external memory can complete the corresponding data manipulation within the prescribed time period in a read/write operation of DSP. DSP does not need to insert the waiting period, and this way is called work mode of zero waiting. This work mode can bring DSP's advantage of high speed into full play. DSP's working efficiency is the highest. In order not to affect DSP's processing speed, it needs access speed of external expansion DSP as fast as possible. The system gets an external a piece of high-speed SRAM-IS6lLV6416 with 64K bytes (64K *16 bit). Its read-write access time is 8 ns in the mode of low power consumption. It can satisfy completely the requirements of zero waiting [20]. As shown in Figure 3, it is connection diagramof IS6lLV6416 and DSP.

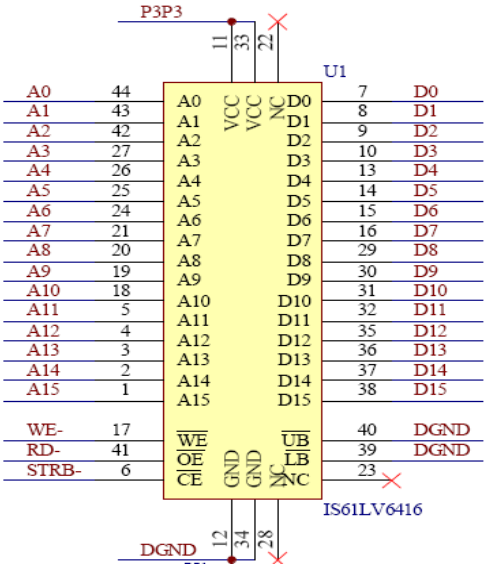

Figure 3 RAM Interface Circuit with DSP External Expansion

JTAG Simulation Interface Circuit. BST-Boundary-Scan Testing is a kind of new testing technology which is put forward with the aim of device density, increasing number of I/O ports, signal injection and the bigger and bigger difficulty of aquisition. It is put forward by the organization of the joint test activities. Later IEEE has developed a testing standard for it which is known as IEEE1149. 1 standard. Based on the JTAG interface technology TMS320LF2407 does not need to use the external physical test probe to obtain data when it is working normally. Boundary scan cell can track the pins' signals logically or capture data from the logic signals of device core. It not only has realized the DSP circuit testing but also has realized the simulation function between the simulator and DSP. JTAG simulation interface circuit is shown in Figure 4. In JTAG simulation interface circuit TDI (test data input), TDO (test data output), TMS (test mode select), TCK (test clock input) are standard four signal lines needed for the boundary scan test [20]. The power supply which is needed by JTAG simulation interface circuit is 5 V or 3.3 V.

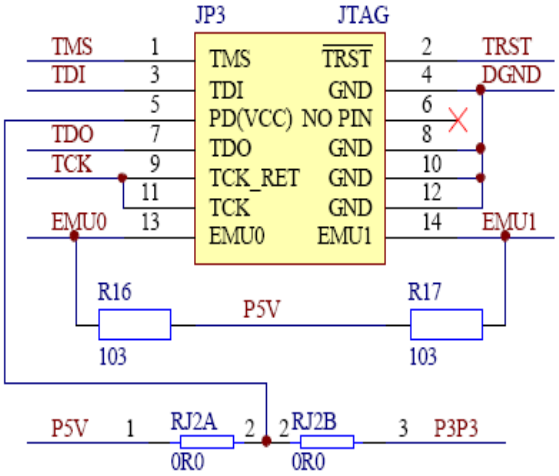

Figure 4 JTAG Simulation Interface Circuit

The Reset Circuit of DSP. This system adopts the reset chip MAX809SD to operate the DSP reset pin $\overline{RS}$ in order to realize the reset operation of DSP chip. The reset circuit is shown in Figure 5. In reset circuit $\overline{RS}$ makes DSP controller terminate its execution and makes PC=0. When we pull $\overline{RS}$ to high level, it starts execution from program memory 0 position. $\overline{RS}$ influences register and status bit. When WDT overflows in periodic time interval, it generates a system reset pulse in pin $\overline{RS}$ [21].

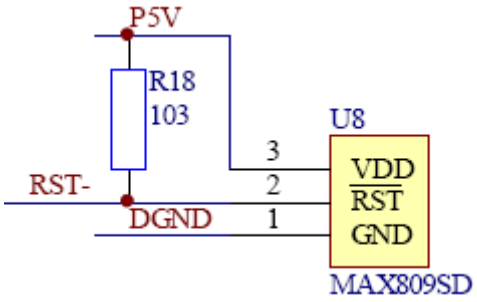

Figure 5 The Reset Circuit of DSP

The Input Pin with the Interruption of DPS Power Drive Protect. When the DC bus current is greater than 25A, when the seventh pin L_OC of operational amplifier TLC2272 7th L_OC changes from high level to low level, the pin $\overline{PDPINT}$ (the input pin with the interruption of power drive protect) is pulled low, it will make an external interrupt at this time. The interruption is provided by the safe operation of the system, such as fast-flowing with the system and other occasions. If $\overline{PDPINT}$ isn't masked, when the pin $\overline{PDPINT}$ is pulled low, all output pins of event managers (EV) are placed by hardware in the state of high impedance. When this event occurs, the interrupted sign associated with $\overline{PDPINT}$ will also be set t to 1. But we must wait that the conversion is determined and synchronized with the internal CPU clock until the interruption can be responded to. This confirmation and synchronization will cause the delay of 3 or 4 CPU clock cycles. If $\overline{PDPINT}$ isn't masked, the interrupted sign will keep EV output be in the state of high impedance and make an interruptible request to DSP kernel. Therefore, as far as the output is concerned, if it must be in the state of high impedance, $\overline{PDPINT}$ must keep the low level of more than 4 CPU clock cycles. The setting of the interrupted signs are not dependent on whether they are masked or not. As long as it create a determined conversion on the pin $\overline{PDPINT}$, everything is ok. $\overline{PDPINT}$ can be used to monitor abnormal information of each state about the system, such as over voltage, over current and too high temperature, etc.

Flash Programming of DSP. When we program on-chip FLASH, we need to pay attention to the setting of software and hardware. We should make MP/ $\overline{MC}$ mode to be selected as $\overline{MC}$ mode,

at the same time the pin Vccp should also be set to high level to allow to program. The related software supplied by running IT on software is ok. But we need to pay attention to that it is better to open the debugger when programming AND make it be in the reset state. And it should make actuating mechanism interrupt current outside the control circuit to prevent a monment's wrong operation in the time of programming from having effects on actuating mechanism. At the same time it can prolong the service life of on-chip FLASH.

The test results

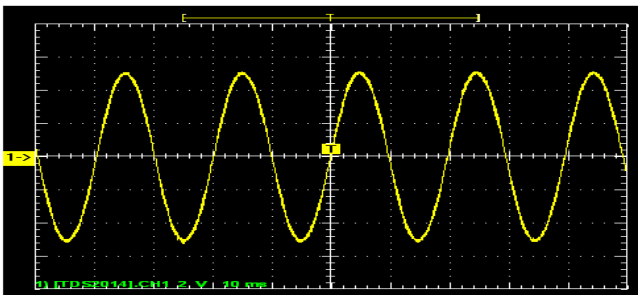

Figure 6 The three phase line voltage intermediate frequency generator main winding for the case of 300V output voltage waveform

As can be seen from table 6, changes in the scope of the main windings three phase voltage is 240~300V, the change range of the DC bus voltage is 336~415V, output voltage effective value can still be guaranteed within the220V + 5%, shown to the DC bus voltage feedforward algorithm good frequency motor speed changes incircumstances, still to ensure the output voltage stability, good for a sinusoidal waveform.

Figure 7a, 7b, 7C to load device with linear output current are respectively 1.2A, 2.5A, 4.5A of output voltage waveform. A, B, C in the three picture, the frequency is 50Hz, the visible frequency of the output voltage is very stable, the output voltage waveform is sine waveform better.

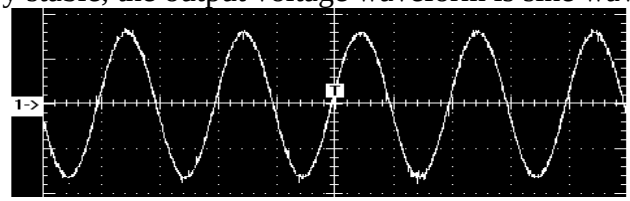

Figure 7a The output current of 1.2A

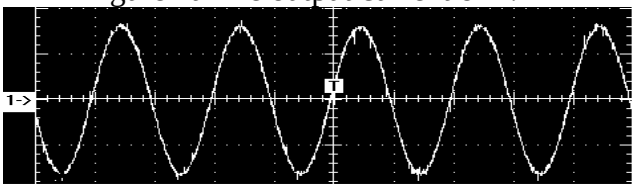

Figure 7b The output current of 2.5A

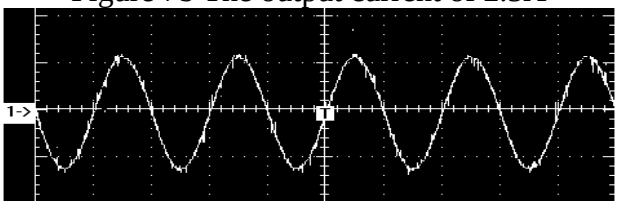

Figure 7c The output current of 4.5A

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