Design and Implementation of Low Power Channel Code for Long Distance Data Transmission

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ABSTRACT: Data transmission channel is the most power consumption part in large scale seismic data acquisition system. In this paper, 9B/10B, a high bit rate channel modulation code is introduced. In order to reduce the implementation complexity, a decoder using direct combinational logic expressions is developed. Its performances based on FPGA is discussed, comparing with the traditional 8B/10B code. Finally, Experiment results showed that a maxim 12% power reduction had been made by using this newly developed channel code.
KEYWORD: 9B/10B; Energy Saving; Seismic Data Acquisition System

1 INTRODUCTION

With the rapid progress of sensor, computer and communication technologies, great achievements had been made in oil exploration industry. Nowadays, large-scale seismic data acquisition system has become a key equipment for seismic exploration. Normally, this kind of system consists of a Central Control Unit(CCU) and several kinds of field units, such as Data Acquisition Unit (DAU) , Power Management Unit(PMU), and Line Management Unit(LMU). The DAU samples the reflected seismic signals and transmits the data upward to the nearby DAU through seismic cable or field line, until it reach to LMU. The LMU is a data management unit for the whole field line it connected, collects all data acquired by every DAU of this line. The PMU provides Power to nearby DAUs and relays the data passing through. The sampling precision will be 24-bit, the valid data speed will be up to 24Mbps in every acquisition line, the data transmission distance will be over 220 meters, and error bit rate (BER) is 10^{-9} at least. A large scale system of this kind will consist tens of thousands of DAUs, several thousand of PMUs. At operation, the whole system will cover several hundred km^2 fields. So it is a very power consumed system.

According to the researchs of this kind of distributed acquisition networks, power consumed in data transmission especially in the transmitting end is more than data acquisition and data processing generally. So, it is very important to develop a simple and reliable modulation scheme and lower the transmitting power as low as possible to maximize the working time of the system. [1]

Optical fiber, which performance in transmission speed and distance is excellent, but it cannot provide remote power supply and its physical characteristic is too weak to be applied in field widely. So optical fiber is not suitable for use in this system. Generally, specific seismic cable is adopted, which is composed by certain pairs of copper Unshielded Twist-Pair (UTP). The specific seismic cable is also strengthened in pulling and pressing characteristics to be applied in field.

This paper aims to reduce the power consumption of the large scale seismic data acquisition system by optimization of data transmission technique. The block diagram of data transmission channel is shown in figure 1.

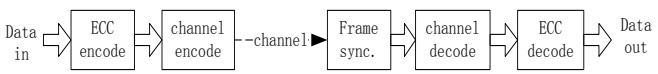

Figure 1.Block diagram of data transmission channel

We will introduce a high bit rate channel codes replacing the former 8B/10B channel code. By reducing the real transmission time through high effective data speed, the power consumption of data transmission channel will be greatly decreased.

2 9B/10B CHANNEL CODE AND ITS FEATURES

In current seismic data acquisition system, 8B/10B modulation code is used as the channel. The 8B/10B code is developed by IBM, converting 8 bit parallel source data into 10 bit serial modulation data. It is a run length limited and DC balanced code, conducive to the clock and data recovery, and is widely used in high speed serial data transmission. However, the coding efficiency of 8B/10B is just 80%, which limits the source data transmission speed.[2][3]

In order to improve the channel code efficiency, we have developed a 9B/10B coding scheme. [4]In this scheme, we convert every 9 bit parallel source data into 10 bit serial modulation data. That is, every 9 bit source code X, which could be expressed as $[x_8x_7x_6x_5\ x_4x_3x_2x_1x_0]$,will be mapped to 10 bit channel code Y with the expression of $[y_9y_8y_7y_6y_5y_4y_3y_2y_1y_0]$. It remains the best features of 8B/10B coding scheme, such as run-length-limited and DC-free, so that it can meet the data transmission requirement of the actual seismic channel, and increase the coding efficiency to 90%.

In the process of 9B/10B coding, the 10B code words selection rules is short run-length priority, which removes all code words with long continuous '0' or '1'bits. The maximum run-length of 9B/10B is 7. Figure 2 shows the run-length distribution of 9B/10B modulation code.

The DC control of transmission channel is realized by selection of the codeword's parity RD-/RD+. The normalized spectrum analysis of encoded channel data flow is shown in Figure 3. The minimum frequency is 0, which represents the DC component. The maximum frequency is 1, which means its transmission period is the shortest channel bit time. It shows that the amplitude of low frequency is very small. So the 9B/10B coding scheme has a perfect DC balance performance.

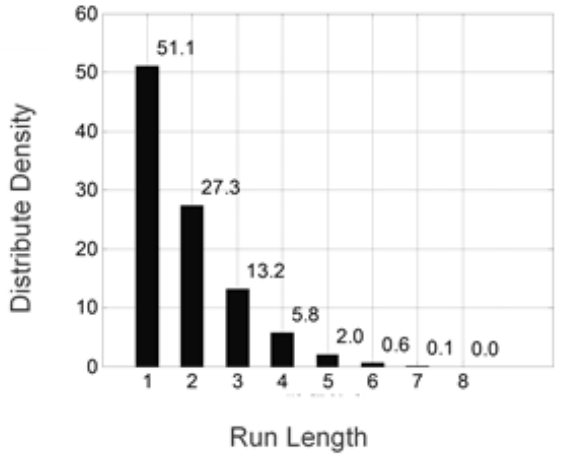

Figure 2. Run-length distribution of 9B/10B modulation code

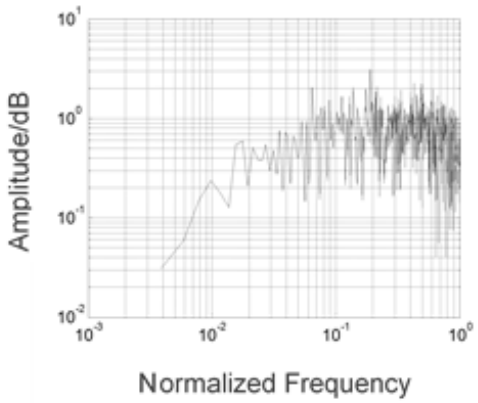

Figure 3. Normalized spectrum analysis of encoded data flow

3 DESIGN, IMPLEMENTION AND VERIFICATION OF 9B/10B CODE

In our large scale seismic data transmission system, the channel modulation encoder and decoder are very important parts of data transmission modular, their performance will directly affect the whole system's bit error rate and power consumption.

Usually, the look-up table method is used for realizing the 9B/10B coding and decoding scheme, which directly maps the 9B source data into the 10B codeword. A great amount of memory will be used to store all possible code tables. When the input data arrives, the controller looks up the memory table, finds out the corresponding codec and finishes the output. The logic design of this method is simple, but the coding and decoding speed is influenced by the complexity of memory operation.

In this paper, we would like to develop the encoder and decoder directly through combinational logic operation based on programmable logical elements in FPGA. The advantage of this method is that the resource cost can be obviously reduced and maximum working frequency can be greatly improved. The most important work of this method is to optimize a set of combinational logic equations of the encoder and decoder. The following shows a group of combinational logic equations for 9B/10B decoder.

$$x_0 = G_1(y_0, y_6) + M_P y_6 + M_N \overline{y_6}$$
$$x_1 = G_1(y_1, y_7) + M_P y_6 + M_N \overline{y_6}$$
$$x_2 = G_1(y_2, y_8) + M_P y_6 + M_N \overline{y_6}$$
$$x_3 = G_1(y_3, y_9) + M_P y_9 + M_N \overline{y_9}$$
$$x_4 = y_4\overline{y_5}A_P + \overline{y_4}y_5A_N + y_4y_5(L_3 + A_P\overline{H_1L_1}) + H_2\overline{L_0}(\overline{y_7}y_9 + y_7y_8) + H_3(y_3 + \overline{y_1}y_2) + \overline{y_4}\,\overline{y_5}(L_1 + H_2L_2(y_7\overline{y_9} + y_6y_9)) + H_1(\overline{y_3} + y_1\overline{y_2})$$
$$x_5 = G_2(y_6, y_0) + M_P + M_N$$
$$x_6 = G_2(y_7, y_1) + M_P y_6 y_7 + M_N(y_8 + y_9)$$

$$x_7 = G_2(y_8, y_2) + M_P\overline{y_9} + M_N y_9$$
$$x_8 = G_2(y_9, y_3) + M_P\overline{y_9} + M_N y_9$$
$$K = y_4 y_5(\overline{y_3} y_6 H_1 L_3 + y_3\overline{y_9} H_3 L_1 + y_2 y_3 H_3 L_2) + \overline{y_4}\,\overline{y_5}(y_3\overline{y_6} H_3 L_1 + \overline{y_3} y_9 H_1 L_3 + y_0 y_1 H_1 L_2) + \overline{y_4} y_5 y_6\,\overline{y_8}\,\overline{y_9} L_4 + y_4\overline{y_5}\,\overline{y_6} y_8 y_9 L_0$$

$$A_N = \overline{H_3 y_4 y_5} L_0 + (y_4 \oplus y_5)(H_1(L_1 + L_2) + H_2 L_1) + H_3 L_3\overline{y_4}\,\overline{y_5}$$
$$A_P = L_4 + (y_4 \oplus y_5)(H_3\overline{L_0} + L_3 + H_2 L_2) + y_4 y_5(H_1(L_1 + L_2) + H_3 L_0)$$
$$B_N = \overline{y_4}\,\overline{y_5}(L_1 + H_1 L_2(\overline{y_0} y_3 + y_0 y_1))$$
$$B_P = y_4 y_5(L_3 + H_3 L_2(y_0\overline{y_3} + y_2 y_3)) + \overline{y_4}\,\overline{y_5} H_2 L_3$$
$$C_N = \overline{y_4}\,\overline{y_5}(\overline{y_6} + y_9) H_2 L_2$$
$$C_P = y_4 y_5(y_6 + \overline{y_9}) H_2(L_1 + L_2) + \overline{y_4}\,\overline{y_5} H_3 L_2$$
$$D_N = \overline{y_4}\,\overline{y_5} y_6\,\overline{y_9} H_2 L_2$$
$$D_P = y_4 y_5\overline{y_6} y_9 H_2(L_1 + L_2)$$
$$E_N = \overline{y_4}\,\overline{y_5} H_1 L_3$$
$$E_P = y_4 y_5 H_3 L_1$$
$$N_N = \overline{y_4}\,\overline{y_5}\,\overline{y_0 \oplus y_3} H_1 L_2$$
$$N_P = y_4 y_5\overline{y_0 \oplus y_3} H_3 L_2$$
$$M_N = \overline{y_4}\,\overline{y_5} y_0 y_2 H_1 L_2$$
$$M_P = y_4 y_5 y_1 y_3 H_3 L_2$$
$$T_1 = B_P L_2 y_6 y_2 + B_N L_2\overline{y_2} + N_P y_7 y_9 + N_N(y_6 + y_8)$$
$$T_2 = C_P H_2 y_6\overline{y_7} + C_N\overline{y_6} y_7 + E_P(y_1 + y_3) + E_N y_0 y_2 + N_P y_8 y_9 + N_N(y_6 + y_7)$$
$$G_1(y_i, y_j) = (A_P + C_P + B_N L_1) y_i + (A_N + C_N + B_P L_3)\overline{y_i} + E_P y_j + E_N\overline{y_j} + T_1$$
$$G_2(y_i, y_j) = (A_P + B_P) y_i + (A_N + B_N + C_P H_3)\overline{y_i} + D_P y_j + D_N\overline{y_j} + T_2$$

In the equations，10 bit channel code [$y_9 \ldots y_0$] will be decoded to 9 bit source code [$x_8 \ldots x_0$]. H_i means the fact that there are i '1' in[$y_9 y_8$ $y_7 y_6$] ($i = 0,1,2,3,4$). L_i means the fact that there are i '1'in[$y_3 y_2$ $y_1 y_0$]. K is the control code identification. If k=1, then the decode word should be a control word, if k=0, then the decode word should be a normal data.

Similarly, we can derive the logic equations of the 9B/10B encoder, however, in order to avoid the tedious, we omitted here the logic equations.

In order to assess the performance of 9B/10B coding scheme, we implement the developed decoder and encoder in an Altera CycloneII EP2C35F484 FPGA, comparing with the traditional 8B/10B encoder and decoder. Table 1 shows the logic resource cost comparison. Table 2 shows the maximum working frequency of the two code schemes.

Table 1 comparison of Logic resource cost

	Encoder cost (LE)	Decoder cost (LE)	Percentage cost of whole FPGA resource
8B/10B	42	39	0.3%
9B/10B	118	121	0.8%

Table 2 comparison of maximum working frequency (MHz)

	Fmax	Restricted Fmax*
8B/10B	170	170
9B/10B	570	340

*Fmax is restricted by the speed of CycloneII FPGA

Table 3 comparison of time cost for data transmission

	5M	8M	10M	12M
8B/10B(s)	42.81	26.75	21.41	17.83
9B/10B(s)	38.21	23.88	19.10	15.92
Time cost rato	1.120	1.120	1.121	1.120

Finally, data transmission experiments have been made using both 8B/10B and 9B/10B schemes. 100000 frames have been transmitted each time with different channel bit rate (5M, 8M, 10M, 12M) and the transmission periods have been recorded. The experiment results are provided at table 3. It shows a 12% transmission time reduction using 9B/10B modulation code, which means that a 12% energy consumption will be saved.

4 CONCLUSIONS

Based on our large scale data acquisition system, a 9B/10B modulation code is introduced in this paper. It is a high bit rate, DC balanced and run-length limited channel code scheme. In order to reduce the implementation complexity, a decoder using direct combinational logic expression is developed. Data transmission experiments showed a 12% transmission time reduction using 9B/10B code, which means that a 12% energy consumption will be saved.

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