One Realization Method of Precise Clock Synchronization Algorithm

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Abstract. This article mainly describes a new approach to realize precise synchronization between master clock and slave clock. To improve the IEEE 1588 synchronization precision, Kalman filtering algorithm is applied based on the application of Ethernet. Four state machines are used to accelerate the process and improve the accuracy of frequency modulation and phase modulation. Simulation result proves that time precision is improved from sub-microsecond to dozens of nanoseconds.

1 IEEE 1588 Principle of Clock Synchronization

IEEE 1588 standard [1] specifies a dedicated protocol that enables precise synchronization of clocks in measurement and control systems implemented with technologies such as network communication, local computing and distributed objects, namely the Precision Time Protocol (PTP). The protocol describes a master−slave relationship among the clocks in the system. Slave clock will change local time to achieve the synchronization with master clock according to the calculated deviation. Basic principle is as below:

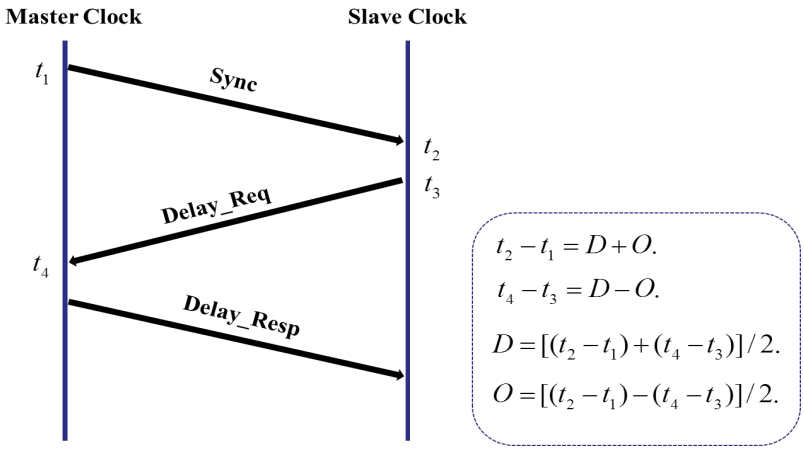

Fig. 1 IEEE 1588 Principle of Clock Synchronization

Timestamps t_1, t_2, t_3, t_4 respectively mean the time when master clock sends a Sync message to slave clock, the slave receives the Sync message, the slave sends a Delay_Req message to the master and the master receives the Delay_Req message. O means the offset between slave clock and master clock, D means time delay. And the precision of time synchronization was mainly affected by noise, which can be divided by system noise and measurement noise.

2 Kalman Filtering Algorithm

2.1 Basic Equation

Kalman filtering algorithm [2] optimally estimates system state of by linear equation of system state based on measured data of system input and output. We introduce one discrete system, which can be described by a linear stochastic difference equation [3, 4].

State equation:

$$X(k) = F(k \mid k-1)X(k-1) + W(k). \tag{1}$$

Measurement equation:

$$Y(k) = HX(k-1) + V(k). \tag{2}$$

Where $X(k)$ is the system state, $Y(k)$ is the measured value. State transition matrix $F(k \mid k-1)$ and measurement matrix H can be calculated. The covariance matrix of $W(k)$ and $V(k)$ is respectively $Q(k)$ and $R(k)$. Meantime, suppose process noise $Q(k)$ and measurement noise $R(k)$ conforms to the law of normal distribution.

Prediction process:

$$X(k \mid k-1) = F(k \mid k-1)X(k-1 \mid k-1). \tag{3}$$

Where $X(k-1 \mid k-1)$ is the best estimated value at state k-1.

Update the covariance $P(k-1 \mid k-1)$ of predicted value $X(k \mid k-1)$:

$$\begin{aligned} P(k \mid k-1) &= \operatorname{cov}(X(k) - X(k \mid k-1)) \\ &= F(k \mid k-1)P(k-1 \mid k-1)F(k \mid k-1)^T + Q(k). \end{aligned} \tag{4}$$

Calculate Kalman gain $K(k)$:

$$K(k) = P(k \mid k-1)H^T \cdot (HP(k \mid k-1)H^T + R(k))^{-1}. \tag{5}$$

Combine predicted value and measurement value, get the optimal estimated value $X(k \mid k)$:

$$X(k \mid k) = X(k \mid k\text{-}1) + K(k)[Y(k) - HX(k \mid k\text{-}1)]. \tag{6}$$

Update the covariance $P(k \mid k)$:

$$P(k \mid k) = [I - K(k)H]P(k \mid k-1). \tag{7}$$

2.2 Equation Solving

Kalman filtering algorithm is used to clock synchronization between master and slave according to the least error principle based on statistical regularities of noise. During the synchronization process, we got 4 timestamps t_1, t_2, t_3, t_4. Suppose state vector $X(k) = (x_1, x_2)^T(k)$, phase difference $x_1 = t_2 - t_1 - D = O$, x_2 means frequency difference. Measurement vector of time state $Y(k) = y(k)$, measurement value $y(k) = t_2 - t_1$, while $H = (1,0)^T$.

According to the meaning of x_1, x_2 and Taylor expansion, state transition matrix:

$$F(k \mid k-1)=\begin{pmatrix}1 & \Delta t\\ 0 & 1\end{pmatrix}.$$

Where Δt represents interval time of two packets.

2.3 Timestamp Selection Algorithm

In order to avoid asymmetry of delay and uncertain environment changes, selecting effective and optimal timestamps is necessary. FPGA [5] hardware implementation method [6] of the timestamp was applied to achieve high precision timestamp for network data. The precision of the timestamp could reach nanoseconds by FPGA programming through VHDL language and adjustable frequency adjustment. The processor can obtain timestamp and insert the corresponding IEEE1588 data frames, and then realize clock synchronization of the whole network.

2.4 State Machine Transition

To accelerate the process and improve accuracy of frequency modulation and phase modulation, four state machines S_1, S_2, S_3, S_4 were introduced. States S_1, S_2, S_3, S_4 are, in order, fast offset, coarse phase modulation, frequency modulation, precise frequency modulation and phase modulation.

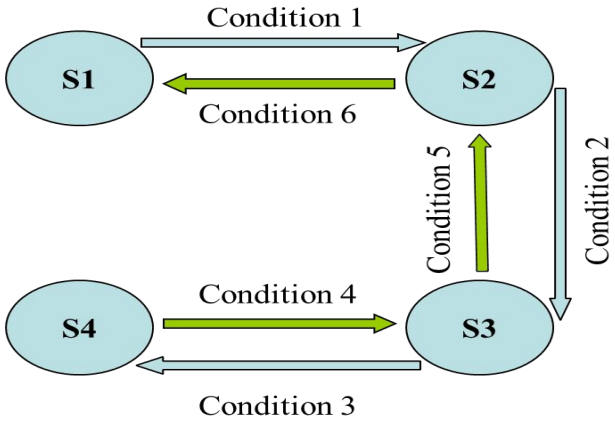

Fig. 2 State Machine Transition

State S_1 will transfer to state S_2 if it satisfies condition 1:

1) $\|x_1\| \le \alpha ms$. Here, α is suggested to 100.

2) State S_1 has run for more than σ times. Here, σ is suggested to 10.

State S_2 will transfer to state S_3 if it satisfies condition 2:

1) If $\|x_1\| \le \beta ms$ runs for two successive times. Here, β is suggested to be 1.

2) State S_2 has run for more than σ times.

State S_3 will transfer to state S_4 if it satisfies condition 3:

1) $\|x_2\| \le \beta us$ for two successive times;

2) State S_3 has run for more than σ times.

For state S_3 and state S_4, we have to avoid unnecessary and multiple frequency modulation and phase modulation. Sometimes, rollback mechanism will be applied when certain situation occurs. State S_4 will roll back to state S_3 if $\|x_2\| > \beta us$ for two successive times, state S_3 will roll back to state S_2 if $\|x_1\| > \beta ms$ for two successive times and state S_2 will be rollback to state S_1 if $\|x_1\| > \alpha ms$ for two successive times.

State machine is designed to accelerate the process and improve the precision of frequency modulation and phase modulation, especially for the application of state rollback mechanism.

3 Simulation Result

Considering the constraint of delay symmetry, I designed the following test topology and made simulation experiment by MATLAB.

Testing device could help capture real-world packet delay variation profiles from existing network and replay those same profiles in a controlled lab environment, enabling to prove 1588v2 products will work in the complex world of Ethernet switches, routers and gateways before deployment.

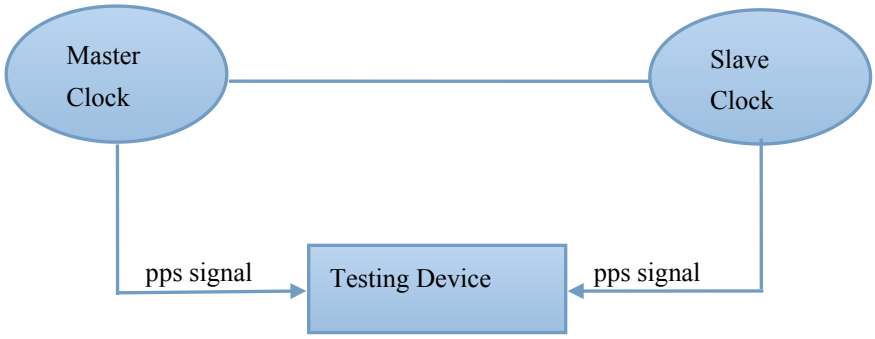

Fig. 3 Test Topology

The key point is to select optimal packets to avoid delay asymmetry. From the following simulation testing result, the Kalman filtering algorithm phase deviation could achieve dozens of nanoseconds.

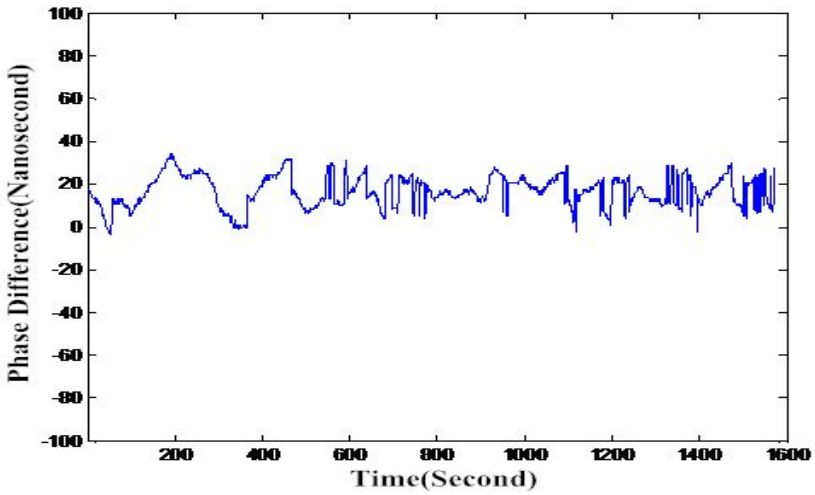

Fig. 4 Kalman Filtering Algorithm Phase Deviation

4 Summary

The paper aims to select optimal packet to narrow the gap between delay from the master clock to the slave clock and delay from the slave clock to the master clock. Kalman filtering algorithm is applied to improve the time accuracy of clock synchronization. The IEEE 1588 time precision is improved from sub-microsecond to dozens of nanoseconds successfully.

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