A multi-chip synchronization system based on diversity technique

Zhang Jun-an[1,2 a *], Li Guang-jun[1], Fu Dong-bing[3], Zhang Rui-tao[2], Yang Yu-jun[3], Wei Ya-feng[2], Liu Jun[2], Li Jiao-xue[2]

[1] Collage of Communication and Information Engineering, University of Electronic Science and Technology of China, Chengdu 611731, P.R China

[2] Science and Technology on Analog Integrated Circuit Laboratory, Chongqing 401332, P.R China

[3]Sichuan Institute of Solid-State Circuits, China Electronics Technology Group Corp., Chongqing 400060, P.R China

[a] zhangjunan2000@sina.com

Keywords: multi-chip synchronization, reliable data receiving, diversity technique.

Abstract. A multi-chip synchronization system based on diversity technique is presented. As diversity technique in communication, at the master IC chip's transmitter, two periodic synchronization signals (with a set delay time between them) have been sent as synchronization reference. At every IC chips' receiver end, a searching method (by internal state machine) is used to obtain the proper receiving clock for the two synchronization signals' reliable receiving, and the two received synchronization signals and an internal generated synchronization signal will be time aligned, only one of them is sent to reset the internal frequency divider. The two received synchronization signals are also monitored, and if any receiving error occurred, then the system will switch to use the other one or the internal one automatically. This multi-chip synchronization system can achieve a reliable multi-chip synchronization performance.

1. Introduction

High speed digital or mixed signal integrated circuits are always embedded with interpolation or MUX blocks, and many clock signals (with different frequencies) are needed. These clock signals are generated from the highest frequency clock signal's frequency division. When several identical IC chips are used in parallel, and each chip's internal frequency divider has a random initial state (as fck/2 and fck/4 signals at different IC chips in figure1), and that will cause the clock signals become asynchronous. This kind of asynchronization must be avoided at some applications. This paper will discuss this multi-chip asynchronization problem, and give a reliable multi-chip synchronization system solution.

This paper is arranged as follows. Section II briefly reviews the conventional multi-chip synchronization system architecture, Section III presents implementation of this paper's multi-chip synchronization system based on diversity technique. Section IV gives a brief performance evaluation. Section Ⅴ, conclusion.

2. Conventional Multi-chip Synchronization System

Conventional multi-chip synchronization system have two kinds of architectures. The first is one-time reset architecture. As shown in figure 1, after all the IC chips are in operational, an external reset signal is sent to every chip at the same time, and resets all the internal frequency dividers simultaneously [1].The advantage of one-time reset architecture is easy to implement, the disadvantage is that it can reset the internal frequency dividers only once, if the synchronous state is disturbed by some interference to asynchronization, it cannot restore synchronization state unless sent a new reset signal from external.

The second is periodic reset architecture, and figure 1 shows the timing diagram. A periodic synchronization signal (always be the maximum division frequency signal) which is sent by the

master chip, and all the IC chips (includes the master chip) receive this synchronization signal as the synchronization reference, then transform it to periodic reset signal (using a rising edge detection circuit with proper latency), and resets all the internal frequency dividers periodically [2]. The advantage of periodic reset architecture is that it can restore the synchronization state as the next reset signal coming whenever it has been disturbed into asynchronization state.

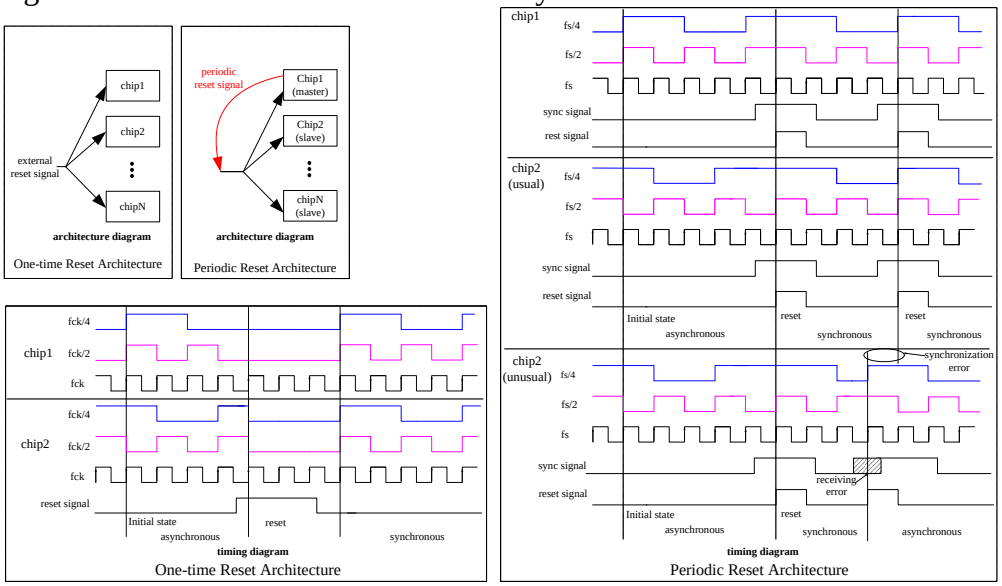

Fig. 1. Two Conventional Multi-chip Synchronization System

As IC chip's clock frequency becomes higher and higher, the periodic synchronization reference signal will be easily disturbed by some interference signal at the PCB board. As shown in figure 1, when the receiving error occurs, it will cause asynchronization at one reset signal period of time. When this kind of error occurs only occasionally, it is not a big trouble. But when this error occurs periodically, it will cause serious problem in some applications.

3. A Multi-chip Synchronization System Based on Diversity Technique

The principle of this paper's multi-chip synchronization system is that let the master chip sends two periodic synchronization signals (with a set delay time between them), and all IC chips receive these two synchronization signals with proper receiving clocks (which are obtained by every IC chip's internal state machine). The two received synchronization signals and an internal generated synchronization signal are aligned in time, and only one of them is sent to the internal frequency divider. A monitor is used to monitor the two received synchronization signals in real-time, if one had a receiving error, then the system will switch to use the other one automatically. If all the two synchronization signals are received incorrectly, the system can switch to the internal generated synchronization signal automatically, and sends an indication signal to let the user known. This method is like the diversity technique in communication.

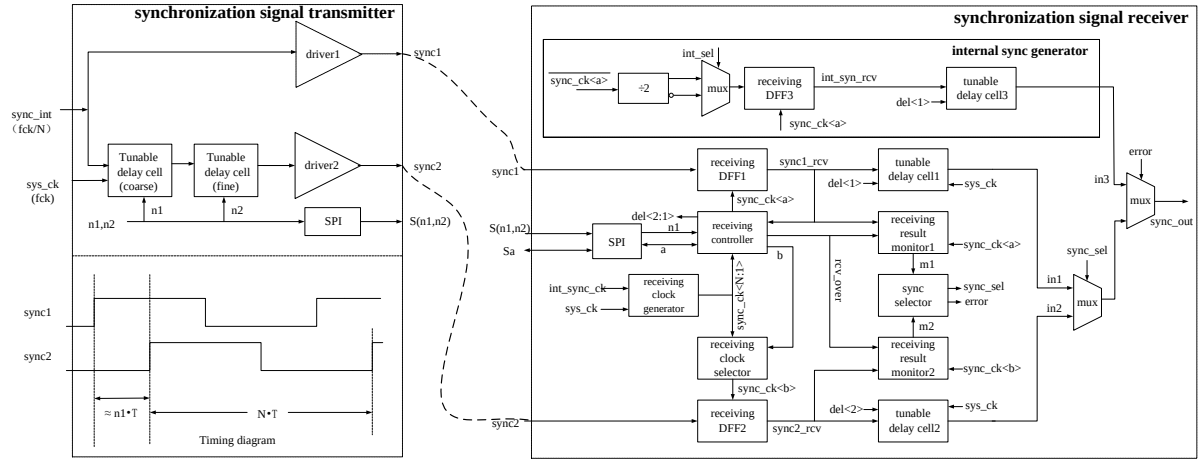

Fig. 2. A Multi-chip Synchronization System Based on Diversity Technique

The transmitter is shown as figure 2, The transmitter sends two synchronization signals as sync1 and sync2 (a set delay time about n1 • T between sync1 and sync2). The sys_ck signal is the highest frequency clock signal (frequency as fck, period as T), sync_int is the internal synchronization signal (fck/N, N is the largest frequency division number of the IC chip), n1 and n2 are tunable integer. The tunable delay cell (coarse) can delay the input signal with the time of n1 • T, and the tunable delay cell (fine) can delay the input signal with the time less than T/2, and n1, n2 also be sent out by an SPI interface.

The receiver is shown as figure 2. The receiving clock generator shifts the in_sync_ck signal (period as $N/2 \cdot T$) to a group of signals as sync_ck<N:1> by using N stages DFFs (two adjacent outputs have a constant delay of T), and the timing diagram is shown as figure 3.

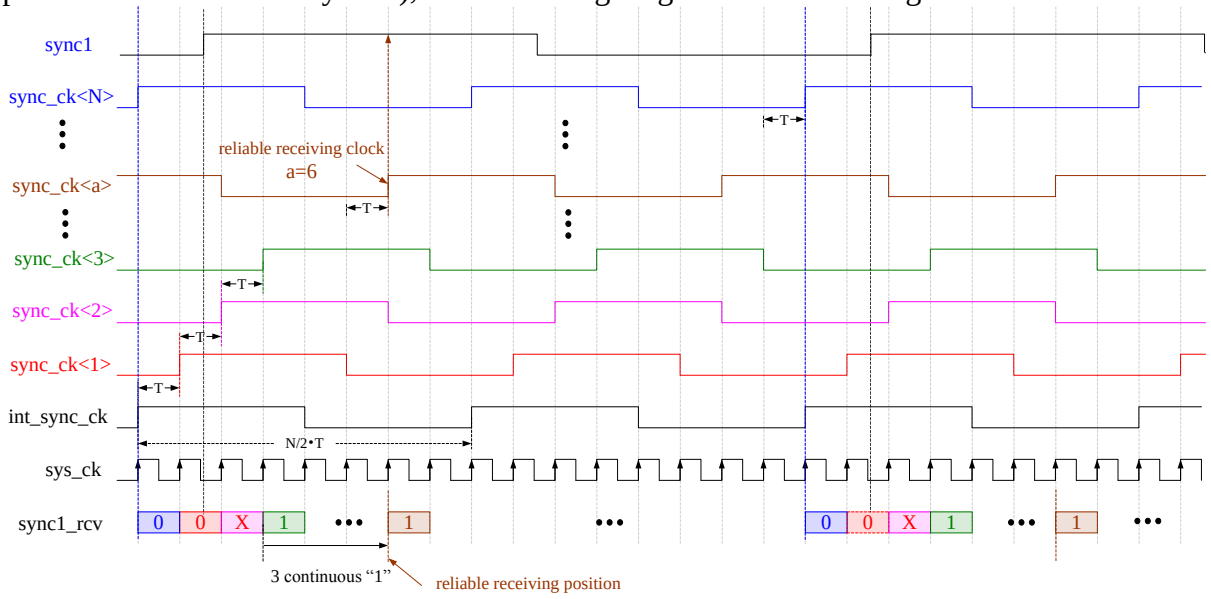

Fig. 3. Time Diagram of the Reliable Receiving Clock Searching

The receiving controller lets each one of the sync_ck<N:1> signals in turn as the clock signal of receiving DFF1 to receive sync1 signal with a fixed number(M) of times, so every sync_ck signal have gotten M receiving results. As shown in figure 3, the receiving result of sync_ck<2> is "X"that means the receiving clock sync_ck<2> is in sync1's unsteady range. an arbitrator is used to select the more appeared result as the final result.

As shown in figure 3, from the N final arbitratored results (by sync_ck<N:1> signals), chooses sync_ck<a> as the proper receiving clock of sync1 because the receiving results have appeared 3 continuous "1", that means the rising edge of sync_ck<a> is definitely in the steady range of sync1. As

this process is over, the receiving controller outputs a rcv_over signal. The different "X" states may cause a time deviation of T between different IC chips, but this small constant deviation is acceptable at most of applications. The user also can tune the value of "n1" and "n2" in the transmitter by SPI interface to avoid this deviation manually.

Depending on sync_ck<a>, sync2 signal's reliable receiving clock sync_ck<b> can be obtained directly. There was a delay time n1 • T between sync1 and sync2, once the integer "a" has been confirmed, let b=a + n1 + N/2. If the obtained "b" is larger than N, the carry will be abandoned. The receiving clock selector chooses sync_ck<b> as the clock signal of receiving DFF2.

As shown in figure 2, an internal sync generator is used to generate an internal synchronization signal (in3). The int_syn_rcv signal has exactly the same frequency and phase with sync1_rcv singal. The int_sel signal depends on the states of rcv_over, sync1_rcv and int_rcv at the initial process of determining, then it is fixed.

The sync1_rcv, sync2_rcv and int_syn_rvc signals will be time aligned by utilizing tunable delay cell 1~3. Depending on "a" and "b", the delay control signal del<1> and del<2> can be obtained. Let del<1> = N - a， del<2>= N-（b-N/2）. If the obtained del<1> and del<2> are larger than N, the carry will be abandoned. The in1, in2 and in3 signal are exactly the same after time alignment.

The sync1_rcv and sync2_rcv will be monitored by receiving result monitor1 and receiving result monitor 2. The correct results of sync1_rcv and sync2_rcv are continuous "0/1"sequences, so it can use an XOR gate to compare the current result with the previous one, if they have the same value that means a receiving error is occurred. The m1 and m2 are indication signal.A sync selector and two 2 to 1 mux can be used to switch the correct received result to the sync_out depended on m1 and m2. Either sync1 and sync2 signal has receiving error, the other will be switched as sync_out signal which is used for the frequency divider's reset. If sync1 and sync2 signals all have receiving errors, the indication signal error will become active, and then the internal synchronization signal(in3) will be switched as sync_out signal. The switching moment must be properly designed to let the synchronization state cannot be interrupted.

4. Performance Evaluation

This multi-chip synchronization system can achieve more reliable performance. When a periodic interference signal (the frequency is lower than fck) in the PCB board which may disturb synchronization signal's receiving, the user can tune "n1" and "n2" at the transmitter, and let at least one synchronization signal will not be disturbed. When an occasional strong interference signal which disturbed all the two synchronization signals at a burst of time, the system can switch to use the internal synchronization signal automatically, and sends an indication signal to let the user known. This switching will not interrupt the IC chip's normal operation. The reliable receiving clock searching method has always been effective when the system clock frequency is changing, this is better than the programmable analog delay line method which may cause out-of-range or insufficient searching range [3]. Synchronization reference signal's frequency of this paper is low (the maximum division frequency as the conventional periodic reset architecture), so the possibility of incorrect receiving is low, and this method is better than literature [4] which is based on the spread spectrum technique.

5. Conclusion

This paper presented a multi-chip synchronization system based on diversity technique. Three periodic synchronization signals can be switched automatically to deal with different kind of external disturbing. In the future, this system can be optimized for some automatically tuning method which can utilize the tunable delay cell (fine) in the transmitter, to deal with the received "X" state in the receiver, and to avoid the possible constant time deviation of T between different IC chips.

Acknowledgment

This work is supported by National Natural Science Foundation of China (No.61006027, No.61176030), Research Foundation of Science and Technology on Analog Integrated Circuit Laboratory (No.9140C0902120C09034, No.9140c090204130c09042), and Fundamental Research Funds for the Central Universities of China (No.ZYGX2012J003).

References

[1] MD652D's datasheet, Euvis, (2006)

[2] AD9910's datasheet, Analog Device, (2007).

[3] Bernd Schafferer: U.S. Patent 6774823 B1 (2004).

[4] Yunchu Li, Engel, Schafferer: U.S. Patent 7933315 B1 (2011).