A Novel Design for Video Frame Switching Based on SoC

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Abstract. In order to solute the problem in existence multi-channel video switch system that the picture may be partly broken at the moment of switching which is a disadvantage in video monitoring, this paper provides a multi-channel video frame switch system in SoC which can upgrade the integration of the circuit and simplify the designing flow and reduce the system cost at the same time. It can be seen from the simulation results that disturbance duration is only one hundred thousandth of an image at the switching moment.

Introduction

Presently, those used in embedded systems video surveillance system mostly are single channel video surveillance model. So, multiple systems can only be purchased in order to conduct multi-channel monitoring. For example, if set up multiple systems in a vehicle installing wiring will be very cumbersome; and equipments will occupy a large space which leads to high costs at the same time. If the requirements changed you must replace the entire system, which is not conducive to upgrade equipment. Moreover, existing video switching mostly are based on time. That is, video signal is switched at regular intervals. Although the control of this switching method is simple but the disadvantages are also obvious. It is not necessarily the switching time of two images in switching moment. In fact, more often, the switch is in the middle of a frame, and then the image quality will be quite unreliable at the switching moment. And there will be half frame images, screen black and screen blurred, which will result image distortion that is not conducive to monitoring and obtain evidence. To solve the above problem we design a frame switching system for multi-channel video signal based on SOC which can ensure the integrity of the image in switching moment of multi-channel video signal[1,2,3].

Switching System Structure Based on SoC

This system receives analog video signals from cameras and the signal is turned into digital signal through the video AD chip and processes digital signal using CPLD/FPGA and outputs the selected video signal. The overall structure of the system is shown as fig. 1.[4]

In the digital image signal encoded in YUV format each frame at the beginning is odd field and the vertical sync signal is high level, which can be used to accurately determine the beginning of the image. In this system structure we use the CPLD/FPGA to catch the start signal of each channel video image and outputs some channel video image according to the selection signal.

This system uses the SCM to set video A/D chips at each boot, and the MCU IP core is integrated in the FPGA/CPLD internal so as to form SoC. Thus, this will not only improve the system's integration and stability while also reducing the system costs[5].

System Implementation

In the actual design, we use 4 channel analog video inputs and the video standard is PAL-D. Analog signals are converted to digital signals by video A/D chip and then enter the FPGA chip for multi-channel signal switching. Finally, the video signal selected is output through the data bus.

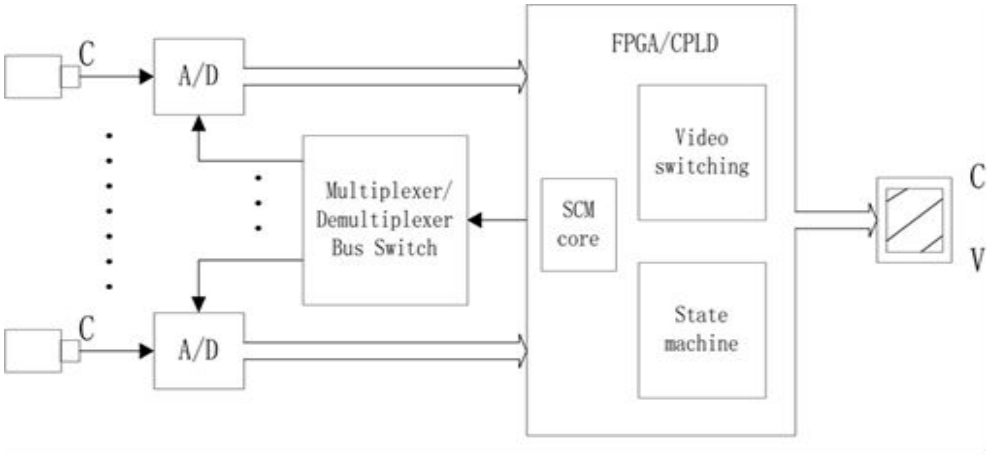

Fig. 1 System structure

Select Device. The video A/D converter chip selected is TVP5150 which supports NTSC/PAL/SECAM formats and can receive two composite video signals input or one S-Video signal and its internal register can be set through the I2C bus, which is completed by the FPGA internal 80C51 IP core. Moreover, because the I2C bus supports only two devices online, therefore use a Multiplexer/Demultiplexer Bus Switch chip so as to the 80C51 IP core can set four video A/D chip through one I2C bus.

Moreover, the FPGA is Cyclone Ⅱ EP2C70 which supports 4 programmable phase-locked loop; provides a flexible clock management and frequency synthesis; contains 150 multiplier (18*18bit) that can perform basic DSP processing; supports differential and single-ended I/O standard; provides 622 pins to users; has fast serial configuration time less than 100ms and can be used for video, image processing and wireless infrastructure design [6].

Video Signal Switching Module Design. According to the signal output timing of TVP5150 we set four states for each input video signal defined as follow:

State_1: Transfer readiness. In this state the state machine waits for the video start signal. Once the state machine captures the signal its state will turned into the next state, otherwise, stays in State_1.

State_2: Odd field image transfer. In this sate system transfer the odd field image data and when the oddeven field detection signal is even field state, the state machine enters the next state, otherwise, stays in State_2.

State_3: Even field image transfer. In this state system transfer the even field image data and when the image tail is detected the state machine enters the next state, otherwise, stays in State_3.

State_4: Transmission end. In this state the image stops transmission, and if the line select signal is received the state machine would enter state_1, otherwise remain in State_4.

The flow chart of the state transition is shown in Fig. 2. Where, SELECT is selected line signal and high level is selected; VSYNC is vertical sync signal and active high; FID is odd-even field data detection signal, and high level is odd field, low level is even field; TAIL is the end flag of the image data and active high.

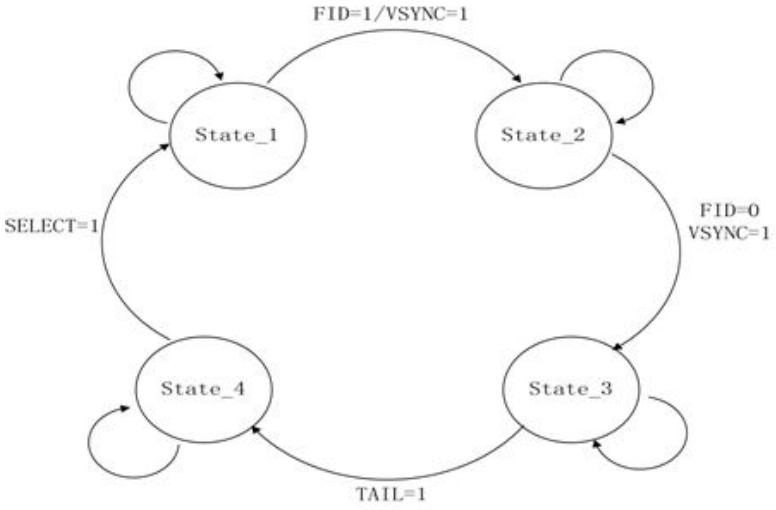

Fig. 2 state diagram

Experiment Simulation

The simulation results in development environment QuartusII6.0 is shown in Fig. 3. YOUT is output signal. And in order to facilitate observation video signals is simple random signal instead of the actual video signal. It can be seen from the figure that the process is still transmit the first signals after activation of the third video signal; the current state of the first video is state three at the frame 2 time but the next state is state four; at the frame 3 time, the current state is state four, and since then, stop the transmission of the video signals. During this process the third way video signal is into the state one for transmission. After the program stop transmission signal the output is high- impedance state and began to transfer the third signals in a short time, and within the short time the system can adequately area two input video signals without disturbing each other. Moreover, it is not appear that during the process of transferring an image to start to transfer another frame image data and reduce effectively reduce the image distortion at the switching moment. In short, the output image quality is better than the traditional video switching system based on time.

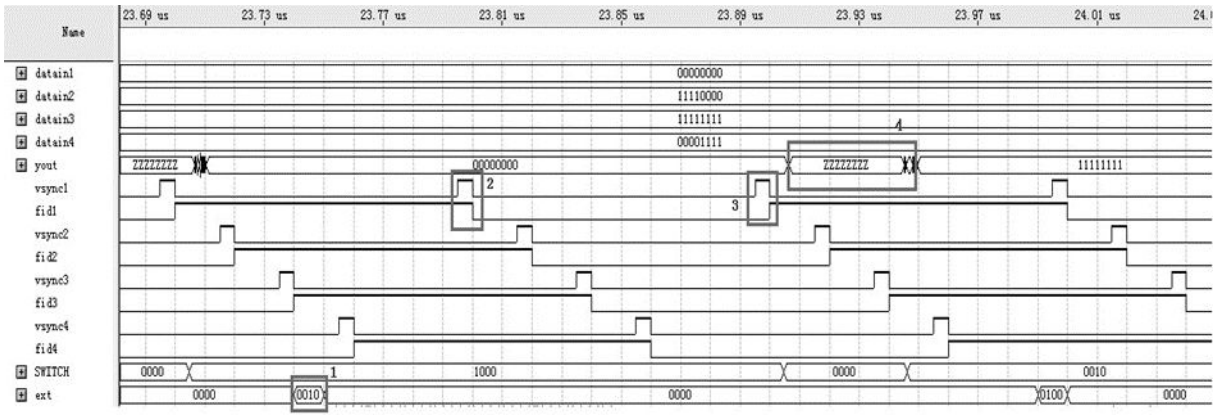

Fig. 3 Simulation results

Conclusion

In this design, the system begin to transfer the image data only when the frame head of the image is detected, so can ensure every frame is complete, which considerably reduces the image distortion problem. Moreover, the system structure based on SoC improves considerably the system integration and implementation efficiency, at the same time, with the greater upgrade capacity it can easily adjust the output time of each channel image automatically or manually. Compared with the widely used

time-based switching system the output video data of the system provided in this paper is more stable and reliable.

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