PC/104 Embedded Computer Module Design Based on SPARC V8 Processor

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Keywords: Embedded Computer, PC/104, Domestic processor, SPARC V8

Abstract: With the development of the computer technology, microelectronics technology and network technology, embedded-systems are widely used in many fields including industry control, railway locomotive control, and vehicle, etc. This paper proposes a hardware design scheme of PC/104 embedded computer module based on SPARC V8 processor which consists of several sub-modules including CPU , PC/104 bus, USB controller and Ethernet controller, etc. In this paper, we present and analyze the detailed design of system level architecture and the sub-modules of PC/104 module. It has a certain reference and guidance significance to further promote the application of domestic processor in various industries.

Introduction

SPARC is a CPU instruction set architecture (ISA), derived from a reduced instruction set computer (RISC) lineage. As an architecture, SPARC allows for a spectrum of chip and system implementations at a variety of price/performance points for a range of applications, including scientific/engineering, programming, real-time, and commercial [2]. The processors based on SPARC architecture have the following features: (1) Few and simple instruction formats. (2) Adopting hard-wired control logic. (3) High processing capacity and reliability [6]. Many domestic companies and universities have launched the research and application of SPARC microprocessor in the aerospace field. How to build the environment of the software and hardware of the microprocessors based on this architecture is worthy studying.

As a kind of common industrial computer bus standard, PC/104 is defined for industrial control especially embedded system control, which is mostly used for management control and data transmission in the fields of aeronautical and space because of its small size, low power consumption and software universality. So it is significant to research the embedded computer module based on the V8 processor and PC/104 bus. This paper mainly studies the hardware design scheme of the embedded computer module which is compatible with PC/104 specification. The PC/104 module is equipped with a domestic processor of SPARC V8 architecture as the CPU and implements the following functions including the friendly human-machine interface, the high-speed data acquisition unit, the USB communication sub-module and Ethernet communication sub-module. In this paper, we have applied structured and modular philosophy to design the hardware, which leads to brisk the hardware platform structure and makes it easy to extend or cut. It can provide a general hardware platform for the development of the intelligent instrument with different functions.

Structure Design

PC/104 embedded computer module uses the high-performance embedded domestic processor based on the SPARC V8 architecture, which has been applied in many aerospace products. The computer module supports the 16/8 bit mode of PC/104 bus. It contains a 128MB SDRAM, a 128MB FLASH memory, 4 RS232 serial communication ports, 2 10M/100M adaptive Ethernet ports, 2 USB

ports and a VGA display port with 1600*1200 display resolution. In this PC/104 module, we have configured VxWorks operating system including BSP, USB keyboard mouse driver, Ethernet driver, UART driver, TFFS file system and other software driver [1]. Drivers are designed for the corresponding hardware devices, such as USB, Ethernet, UART and display control circuit to manage the underlying hardware, which can provide a standardized and hardware-independent interface to the high-level application software. Fig. 1 shows the main block diagram of PC/104 embedded computer module.

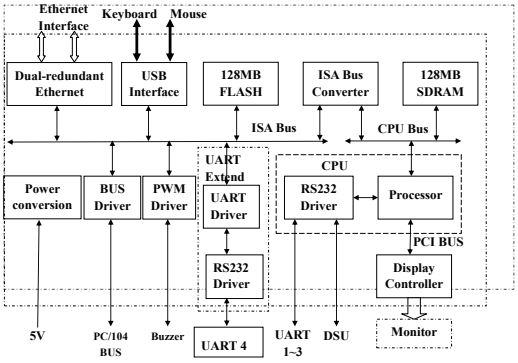

Fig. 1 The main block diagram of PC/104 embedded computer module

Hardware Module Design Based on Domestic Processor

CPU Sub-module

A 32-bit microprocessor based on SPARC V8 architecture with the high degree of integration and high performance is adopted in this design. Fig. 2 shows the internal structure of the processor. From Fig. 2, we can see the processor chip contains an on-chip integer processing unit IU, a floating-point unit (FPU), independent data caches and instruction caches, 5 stage pipeline, hardware multiplier and divider and so on. Moreover, interrupt controller, hardware debug unit with tracking buffer storage (DSU), two common timer (timer0, timer1), serial interface, PCI interface, watchdog timer and memory controller supporting PROM, SRAM, SDRAM and I/O space accessing and so on are integrated in this processor chip[4].

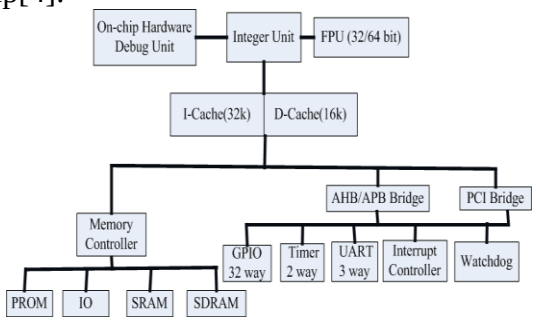

Fig. 2 The structure diagram of SPARC V8 CPU

PC/104 Bus Sub-module

The electrical logic of PC/104 specification uses ISA bus specification. It defines two types of address space including I/O space and memory space, supporting 8-bit and 16-bit data accessing. The hardware of PC/104 can configure 11 interrupt sources and provide 7 DMA Channels. Due to the characteristics of V8 processor chip, in the designing of PC/104 module, we use dual space mapping mode to support the 8/16 read-write functions of PC/104 bus. The I/O space of V8 processor has the following two regions:

(1) One region is used to deal with the 16-bit read-write functions of PC/104 bus, which can be divided into two subspaces, namely I/O space and memory space. The PC/104 bus accessing operations to this space are all considered to be 16-bit read-write mode. In this region, the MEMCS16# and IOCS16# signals are all ignored (assuming the device accessed is 16 bits).

(2) Another region is specifically designed for 8-bit read-write functions of PC/104 bus, which can also be divided into two subspaces, namely IO space and storage space. The PC/104 bus accessing operations to this space are considered to be 8-bit read-write mode. The accessed device is served as an 8-bit device or a 16-bit device by the MEMCS16# and IOCS16# signal and the PC/104 data bus is mapped into the corresponding space of the processor.

In order to improve the efficiency of bus accessing and the controlling flexibility, we implement the bus sequential control logic circuits on a FPGA chip. Through this designing method, the PC/104 bus sequence can be set flexibly by configuring the software, for example, the length (T1) of the address latch signal (BALE) or the default length (T2) of the bus access cycle can be changed by modifying the control register. The PC/104 bus sequence waveforms are shown in Fig. 3. In this figure, the term T4 is the time gap between the BALE falling edge and read-write signal falling edge, which has a minimum value of zero.

As shown in Fig. 3, the length of T1 can be set by the BALEW domain of PC/104 bus sequence control register (ISATIMING). The length of T4 is 0~10ns. The length of T3 is T2-T1-T3. The default value of T2 is set by the ISAW domain of ISATIMING register.

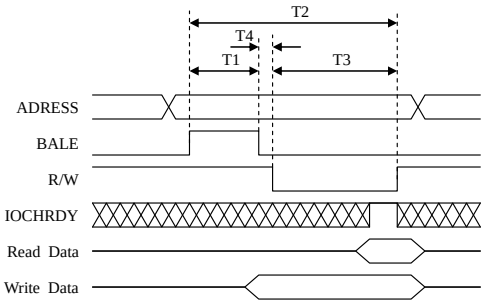

Fig. 3 PC/104 bus waveform Diagram

USB Sub-module

In this paper, we use CH374U (produced by Nanjing QinHeng Electronics Co.,Ltd.) as the USB controller of PC/104 embedded computer module and implement two USB1.0 ports (usb0, usb1), which can connect keyboard, mouse, or the other USB external devices. The interface of USB adopts PulseGuard ESD protection circuit to implement the over-voltage protection. CH374U supports both USB-HOST and USB-DEVICE mode with root hub of 3 ports. It has multiple transmission method, including low speed and full speed control transmission, bulk transmission, interrupt transmission, and synchronous transmission. CH374U uses four I/O registers to interact with the CPU and can generate an interrupt request to CPU. The four registers are all adopted 16-bit accessing mode, but only low 8 bits are effective. High 8 bits are read with constant zero and writing in is arbitrary. The hardware block diagram of USB is shown in Fig. 4.

Fig. 4 USB signal connection diagram

Ethernet Sub-module

The two-way 10M/100M adaptive Ethernet interface (LAN1, LAN2) is implemented with the module using DM9000CIEP owned by Davicom Semiconductor, Inc. In order to improve the reliability of the internal work of the PC/104 embedded computer module, the double isolation interface scheme is adopted in the Ethernet interface, namely the input and output signals separated by the transformer. Two way Ethernet interfaces can work independently and also can be redundant backup for each other used under the driver management [5]. The hardware block diagram is shown in Fig. 5.

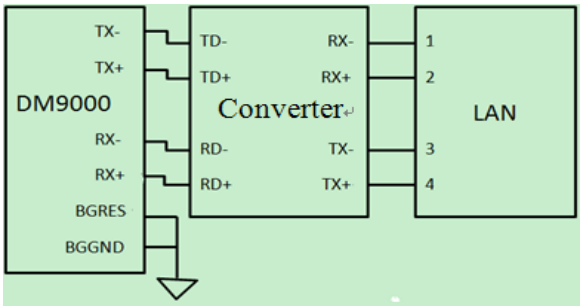

Fig. 5 Ethernet signal connection Diagram

Test results

The cast plate is made according to the above design and the module real figure is shown in Fig. 6. The PCB boards are put to the test and the tests are mainly about the validity of the various functions modules of the PC/104 embedded computer module. The tests are mainly as follows：

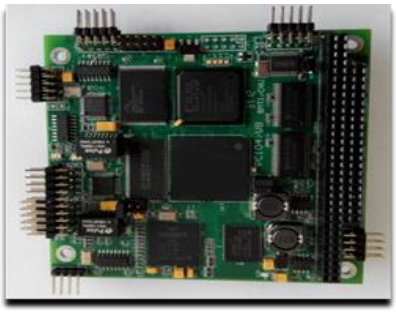

Fig. 6 Module physical Diagram

(1) CPU functional testing, the main function is to test the cache, perform the same cycle, it is 19us to open the cache code, 195us to close the cache code time.

(2) In order to test the PC/104 module more fully, we design a motherboard with a CPLD chip which implements several registers including ISA bus interrupt request control register, accessing latency control register, clock-timing registers. The V8 PC/104 computer module can access these functional registers by internal ISA bus in order to control the CPLD to generate the bus interrupts or modify the bus latency. Using these control method, we can implement the test of PC/104 module.

The generation and clear of the PC/104 bus interrupt signal is controlled by the interrupt request register and the interrupt enable register, which is how the bus interrupt signal is tested.

The bus access cycle controller is mainly to test the validity of the bus access after inserting the different length of wait states the maximum of which is 256us. These waiting for the cycle controllers is only effective for testing the functional registers (IO address 0000 ~ 00FFH). The signal IOCHRDY is in the state of high resistance and the default cycle is adopted while the registers are accessed by other ISA address.

The timer is set with a kind of bus clock when the clock timing is tested. And firstly the 33MHz (CPLD operating clock), 14.318MHz (bus BCLK clock), 14.318MHz (bus OSC clock) are respectively divided into 1MHz by an internal frequency divider, and then the signal is stipulated-timing-controlled by a set of registers. When it comes to overflowing in the timer, the interrupt request is applied to the ISA bus by the interrupt request signal (IRQ12, 14 or 15). And the timer can be tested by software reading the timer count.

(3) Ethernet communication test: Two way Ethernet are connected to the test monitoring computer with the router. Ethernet transferring the data is normal and the average transfer rate is about 1Mbps, and the error rate is zero, and the packet loss rate is zero.

(4) In the operating system, SDRAM memory which is not occupied by the operating system is accessing tested. In order to accurately test the validity of the data bus, writing-in data must have wide adaptability, including 0x55555555、 0xaaaaaaaa、 0x1、 0x2、 0x4、 0x8、 0x10、 ……、

0x80000000. The data in two formats is mainly tested for reading the preliminarily stored data in the FLASH memory. One is the binary data stored in the space that is not changed into the file system, the other is a file stored in the file system, and the test results are correct. Display images and memory access test: After receiving the test command, the specific graphics display functions are called so that the specific graphics can be displayed on the display and the read and write accessing to the display buffer memory is normal. In the RS232 communication test, four RS232 interfaces of the V8 PC/104 computer module are two-two interconnected to send and receive data, and serial data transmission is normal, and the average Baud rate is about 90kbps, and the error rate is zero.

Conclusions

The embedded system has been widely used in the field of industrial control, such as industrial process control, intelligent instrument, and numerical control system. Especially with the network technology and communication technology rapidly booming, the networked site of the industrial control has become a trend. In this paper, after studying the development situation of the embedded system at home and abroad, the relatively complete solution to the embedded application system is designed with a high-performance domestic embedded processor based on SPARC V8 architecture. And the 128MB bytes of FLASH that is used to store all the program codes and parameters is extended in this system and the 128MB bytes of SDRAM that is used to store running programs and data is extended in this system and PC/104 bus is extended in this system to improve the efficiency of bus access and control flexibility. Moreover, USB, Ethernet communication interface and etc. are designed in this system. The testing results indicate that the function indexes and performance indexes meet the requirements. This module is featured in a small size, powerful functions, low power consumption, high reliability, good compatibility and low cost [3], which means it can be applied in different fields of the industrial occasions.

Acknowledgments

This work was supported in part by the National Natural Science Foundation of China (No.61170009, No.61472260, No.61402302); Beijing Natural Science Foundation of China (No.4132016, No.4143060); the Project of Construction of Innovative Teams and Teacher Career Development for Universities and Colleges Under Beijing Municipality(No.IDHT20150507); the Scientific Research Base Development Program of the Beijing Municipal Commission of Education.

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