Z-domain Analysis about the Impact of Op-Amp FDCG, NLDCG, GBW and SR on Performance of Switched-Capacitor Integrator

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Abstract. The corresponding variation form of the Z-domain transfer function of switched -capacitor integrator(behavioral simulation model) under the impact of op-amp's four nonlinearities are explored in detail in this paper, which are finite direct-current gain(FDCG), nonlinear direct-current gain(NLDCG), slew rate(SR) and gain-bandwidth product(GBW) respectively. It's assumed that the integrator is free from the effect of SR and GBW when dealing with the FDCG and NLDCG, namely, in other words, the sampling and integrating can be finished in a very short time slot. Then based on the total charge conservation in sampling capacitor and integrating one, we find out the relationship between the input and output of the switched-capacitor integrator. After that, the relational expression is further translated into the Z-domain model. Especially, when looking into the effect of the finite SR and GBW, in order to establish the zero-input response during integration phase, we convert the issue into the zero-status response of the equivalent step input utilizing the equivalence principle between the charge and discharge of the sampling capacitor. In such a way, the complexity of the analyzing and calculating is effectively simplified. The presented mathematical analysis in this paper is the theoretical foundation of behavioral modeling and simulation for op-amp's four nonlinear properties employing MATLAB/SIMULINK software tools.

1. Introduction

As a significant alternative of electronic system's front-end data collecting and converting, discrete time $\Delta\Sigma$ modulator (Fig.1) are widely applied in such fields as wireless communication, computer, consumer electronics, and so on [1,2]. In earlier stage of the $\Delta\Sigma$ modulator design, system topology, primary specification (such as signal-to-noise-and-distortion-ratio (SNDR), effective number of bits (ENOB), spectral characteristic (such as power spectral distribution (PSD)) need to be predicted and evaluated. They are subject to several non-idealities existing in the system to varying degrees including clock jitter(CJ), excess loop delay(ELD), operational non-idealities, KT/C noise, and so forth. To improve the reliability and feasibility of the prediction, it is necessary to implement precise behavioral modeling, simulation for the whole circuit system. Up to now, research about behavioral modeling and simulation is quite common aimed at switched-capacitor (SC) $\Delta\Sigma$ modulator shown in Fig.2 [3,4], however the mathematical model was usually employed directly, without enough elaborate exploring for the fundamental problem appeared in the literatures. That's why we conduct a research on it. With the addition of op-amp's nonlinearities one after another in the following derivation, the complexity and accuracy of the derived Z-domain model of SC integrator increase progressively.

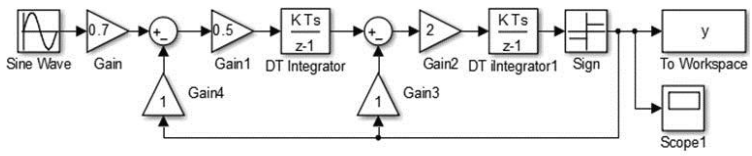

Fig.1 a second order modulator with delayed SC integrator

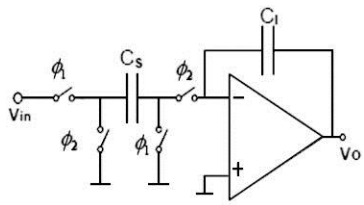

Fig.2 a typical structure of SC integrator

2. FDCG

During integration of the SC integrator in Fig.2, neither the charge on the sampling capacitor c_S move to the integrating capacitor c_I completely due to the op-amp's FDCG, nor the initial charge of c_I is reserved entirely, actually, it offer a portion to c_S. It is assumed that during integrating, the voltage increment of c_I caused by charge transfer form c_S to c_I is v_{o1}. Due to a small fraction of charge transfer from c_I to c_S, the initial voltage of c_I decrease and the new value become v_{o2}, therefore the output voltage is composed of two parts at the end of the nth sampling period, denoted by

$$v_o(n) = v_{o1}(n) + v_{o2}(n) \tag{1}$$

In the course of integrating, the initial charge of c_S is redistributed between c_S and c_I, and the charge conservation equation is as follow

$$c_S v_{in}(n-1) = c_S\, v_{o1}(\mathrm{n})/A_0 + c_I(1+1/A_0)v_{o1}(\mathrm{n}) \tag{2}$$

$$\Rightarrow v_{o1}(\mathrm{n}) = \frac{k_s}{1+(1+k_s)/A_0} v_{in}(n-1) \approx k_s\left(1-\frac{1+k_s}{A_0}\right)v_{in}(n-1) \tag{3}$$

There is $k_s = c_S/c_I$ in the above formula. During charge integration period, the initial charge of c_S is rearranged. Its charge conservation equation is

$$c_I v_o(\mathrm{n}-1) = c_I v_{o2}(n) - c_S v_{\_}(\mathrm{n}) \tag{4}$$

$$\Rightarrow v_{o2}(n) = v_o(\mathrm{n}-1)/\left(1+k_s/A_0\right) \approx \left(1-k_s/A_0\right)v_o(\mathrm{n}-1) \tag{5}$$

Within (4), $v_{\_}(\mathrm{n}) = -v_{o2}(\mathrm{n})/A_0$, Substituting (3) (5) into (1), we get

$$v_o(\mathrm{n}) = k_s\left(1-\frac{1+k_s}{A_0}\right)v_{in}(n-1) + \left(1-\frac{k_s}{A_0}\right)v_o(n-1) \tag{6}$$

$$\overset{z}{\leftrightarrow} V_o(\mathrm{z}) = k_s\left(1-\frac{1+k_s}{A_0}\right)z^{-1} \Big/ \left[1-\left(1-\frac{k_s}{A_0}\right)z^{-1}\right] \tag{7}$$

Set $g = k_s[1-(1+k_s)/A_0]$ and $\alpha = \left(1-k_s/A_0\right)$, Then the transfer function of non-ideal SC integrator become [5,6,7]

$$\mathrm{H(z)} = g\, z^{-1}/(1-\alpha z^{-1}) \tag{8}$$

Wherein g is known as integration gain, α decaying coefficient of integration output, they are both generated by charge leakage during integration resulted from the op-amp FDCG. Actually g isn't the transient (real time) gain. In the first half period when input signal voltage takes effect, the output voltage is immune to it, hence in practice, g is a delayed gain, approximately the ratio of output voltage at the end time of the clock period to input voltage at the initial moment (in general, due to the relatively high sampling frequency, the input voltage within one clock period is regarded as invariableness). As the ratio between the attenuation value of the initial voltage of output terminal after one clock period and itself, α is brought about by the integrator charge leakage.

3. Nonlinear DCG

The op-amp DCG is usually considered as constant in most of SC integrator model. Actually,

owing to nonlinear variation of the drain resistance of MOS transistor at output terminal depending on output voltage v_o, the op-amp DCG vary nonlinearly according to v_o, as shown below [5,6]

$$A_{0,\text{non}} = A_0(1+\alpha_1|v_o|+\alpha_2|v_o|^2+\cdots = A_0\sum_{i=1}^{\infty}\left(1+\alpha_i|v_o|^i\right) \tag{9}$$

It is found that in (2) and (4), $A_{0,\text{non}}$ is the DC gain at the moment of n*Ts, thus

$$A_{0,\text{non}} = A_0(1+\gamma_1|v_o(\text{n})|+\gamma_2|v_o(\text{n})|^2+\cdots = A_0\sum_{i=1}^{\infty}\left(1+\gamma_i|v_o(\text{n})|^i\right) \tag{10}$$

Substituting (9) into the expression of g, α, we obtain

$$g_1 = k_s\left\{1-(1+k_s)\Big/\left\{A_0\left[1+\sum_{i=1}^{\infty}\left(\gamma_i|v_o(\text{n})|^i\right)\right]\right\}\right\} \approx k_s\left\{1-\frac{1+k_s}{A_0}\left[1-\sum_{i=1}^{\infty}\left(\gamma_i|v_o(\text{n})|^i\right)\right]\right\} \tag{11}$$

$$\alpha_1 = 1-k_s\Big/\left\{A_0\left[1+\sum_{i=1}^{\infty}\left(\gamma_i|v_o(\text{n})|^i\right)\right]\right\} \approx 1-\frac{k_s}{A_0}\left[1-\sum_{i=1}^{\infty}\left(\gamma_i|v_o(\text{n})|^i\right)\right] \tag{12}$$

In an optimal situation of infinite op-amp gain, it holds that

$$v_o(\text{n}) = v_o(\text{n}-1)+k_s v_{in}(\text{n}-1) \tag{13}$$

Bringing it into (11) (12), result in

$$g_1 = k_s\left\{1-\frac{1+k_s}{A_0}\left[1-\sum_{i=1}^{\infty}\left(\gamma_i|v_o(\text{n}-1)+k_s v_{in}(\text{n}-1)|^i\right)\right]\right\} \tag{14}$$

$$\alpha_1 = \left(1-\frac{k_s}{A_0}\left[1-\sum_{i=1}^{\infty}\left(\gamma_i|v_o(\text{n}-1)+k_s v_{in}(\text{n}-1)|^i\right)\right]\right) \tag{15}$$

4. Op-amp Finite GBW and SR

The influence of GBW and SR on its value is excluded from the aforementioned integrator gain calculation. Due to the finite values of both, the output voltage can't arrive at the set value merely ensured by charge conservation, but is dominated by an exponential dependence. So its output value is probably less than the value without taking GBW and SR into account. Accordingly it's possible that the real value of the integration gain g and g_1 at the end point of the nth period is smaller than the above calculated value. Since the gain of the op-amp is quite large, there are only a little decrease relative to the initial output voltage $v_o(n-1)$ throughout integration, leading to such a fact that even if it is limited by finite GBW and SR, the initial output voltage can still reduce to the quantity specified by the op-amp FDCG and nonlinearity within a half period integration time. So the output decaying coefficients α and α_1 are unaffected. To confirm the impact of the op-amp's limited GBW and SR on the integration gain, we need to know the transient response of integrator output voltage all through integration.

In the following, the calculation of the transient response of integrator output voltage in integration phase is presented (exponentially establishing process).

4.1 Op-amp gain with intermediate frequency. Let the op-amp has DC gain A_0 and single pole ω_p, then the voltage transfer function can be denoted as $A_v = A_0 / \left(1 + s/\omega_p\right)$. Under intermediate frequency condition $\omega_p \ll \omega \ll \omega_{ta}$, this formula can be simplified as $A_v = \omega_{ta}/s = 2\pi GBW/s$, wherein the unit gain angular frequency is $\omega_{ta} = 2\pi GBW = \omega_p A_0$ [8].

4.2 The composition of the transient response. During the integration phase $[(n-1/2)T_S, nT_S]$, the transient response voltage at the integrator output point is composed of the initial value $\alpha_1 v_o[(n-1)T_S]$ at $(n-1)T_S$ moment and a zero-input response $v_{o,zi}(t)$ (assuming that the variation of the initial voltage at the output end can be finished instantaneously, the meaning of α_1 will be given in the following), namely

$$v_o[t] = \alpha_1 v_o\left[(n-1)T_s\right] + v_{o,zi}(t), \quad t \in \left[(n-1/2)T_s, \ nT_s\right] \tag{16}$$

4.3 The transfer-function within integration phase. Based on the fact that the voltage on c_S induced by input voltage is equal to the one came from output voltage, we have the following relationship

$$V_{C_S}(s) = V_o(s)\frac{1/sc_S}{1/sc_S + 1/sc_I} = V_o(s)\frac{c_I}{c_S + c_I} = \beta V_o(s) \tag{17}$$

Let the integrator input voltage be $v_i(t) \overset{L}{\leftrightarrow} V_i(s)$ during its integration phase, then the voltage of the op-amp's negative input node acts as

$$V_-(s) = V_i(s) + V_{C_S}(s) = V_i(s) + \beta V_o(s) \tag{18}$$

The op-amp output voltage meet

$$V_o(s) = -\left[V_i(s) + \beta V_o(s)\right]A_v \tag{19}$$

Thus the transfer function of the integrator during integration phase becomes

$$A_I(s) = \frac{V_o(s)}{V_i(s)} = \frac{-A_v}{1+\beta A_v} = \frac{-\omega_{ta}}{s+\beta\omega_{ta}} = \frac{-1}{\beta}\frac{1}{1+s/\beta\omega_{ta}}, \beta = \frac{1}{1+k_s} \tag{20}$$

4.4 Zero input response $\mathbf{v_{o,zi}(t)}$. During integration phase, sampling capacitor with zero input discharge, while charging the integrating capacitor c_I. If the initial charge of c_S is set to 0, and put an appropriate step voltage $-V_{s,eq}$ between c_S and ground (whose value will be determined next step), it seems that the voltage span over the two ends of c_S (because there exists an equivalence between the two voltage drops, one from the integrator output to the op-amp negative input, the other from the same point to ground).

Such a way amounts to charge the zero initial status capacitor c_S. As long as the steady states are equal in value of the integrator output voltage under the two conditions of zero state charging and zero input discharging of c_S respectively, the charging and discharging process of c_I are exactly

the same, thus in both cases, the transient variation process of output voltage are also identical. In view of the above consideration, we solve for the zero input response $v_{o,zi}(\mathrm{t})$ of the integrator output point indirectly though seeking zero status response $v_{o,zs}(\mathrm{t})$ to step voltage $-V_{s,eq}$.

As known the integrator input voltage in integration phase is

$$\mathrm{v}_i(t) = -V_{s,eq}u(t) \overset{L}{\longleftrightarrow} V_i(s) = \frac{-V_{s,eq}}{s} \tag{21}$$

So, $V_{o,zi}(s) = V_{o,zs}(s) = V_i(s)\cdot A_I(s) = \frac{-V_{s,eq}}{s}\cdot\frac{-1}{\beta}\cdot\frac{1}{1+s/\beta\omega_{ta}}$

$$= \frac{V_{s,eq}}{\beta}\left(\frac{1}{s} - \frac{1}{s+\beta\omega_{ta}}\right) \leftrightarrow \frac{V_{s,eq}}{\beta}\left(1-e^{\frac{-t}{\tau}}\right)u(t),\ \ t\in[0,T_s/2] \tag{22}$$

Within above equation, $\tau = 1/(\beta\omega_{ta}) = 1/(2\pi\beta GBW)$.

4.5 Equivalent step input amplitude $\mathbf{Vs,eq}$. In integration phase, due to the similar response when discharging c_S as that when charging it based on the assumption of utilizing the step voltage $-V_{s,eq}$, the same stable status values come into being. According to (3) (17) (20), it can be known that

$$V_{s,eq} = \beta g v_{in}(n-1) = k_s\left(\frac{1}{1+k_s} - \frac{1}{A_0}\right)v_{in}(n-1) \tag{23}$$

Between them g is the leakage factor of the integrator output voltage resulted from the initial charge on sampling capacitor c_S.

4.6 Transient response $\mathbf{v_o(t)}$. According to (16) (22) (23), we get [9]

$$v_o(t) = \alpha v_o\left[(n-1)T_s\right] + g v_{in}(n-1)\left(1-e^{-\left(t-\left(n-\frac{1}{2}\right)T_s\right)/\tau}\right)u\left[t-\left(n-\frac{1}{2}\right)T_s\right] \tag{24}$$

In which $t\in\left[(n-1/2)T_s,\ nT_s\right]$, on account of the maximum slope of $v_o(\mathrm{t})$ at the initial time of integration phase, we have

$$dv_o/dt\big|_{\max} = g v_{in}(n-1)/\tau \tag{25}$$

Provided that $dv_o/dt\big|_{\max} \le SR$, the output response of the integrator is dominated by (24), while under $dv_o/dt\big|_{\max} > SR$ circumstance, the output vary along with the next piecewise function [9]

$$v_o(t) = \begin{cases} \alpha v_o\left[(n-1)T_s\right] + SR\cdot\left[t-\left(n-\frac{1}{2}\right)T_s\right], t\le t_0 \\ v_o(t_0) + \left[g v_{in}(n-1) - SR\cdot t_0\right]\left(1-e^{-\left(t-\left(n-\frac{1}{2}\right)T_s\right)/\tau}\right)u\left[t-\left(n-\frac{1}{2}\right)T_s\right], t>t_0 \end{cases} \tag{26}$$

In above expression $t_0 = \ln\left[SR \cdot \tau / g v_{in}(n-1)\right] + \left(n - 1/2\right)T_s$, Let $t = nT_s$ in (23) (25), the following is obtained respectively

$$v_o\left(n\right) = \alpha v_o\left[\left(n-1\right)T_s\right] + + g v_{in}(n-1)\left(1 - e^{-T_s/2\tau}\right)$$
$$\overset{Z}{\leftrightarrow} \mathrm{H(z)} = V_o(z)/V_{in}(z) = g\left(1 - e^{-T_s/2\tau}\right)z^{-1}\Big/(1 - \alpha z^{-1}) \tag{27}$$

$$v_o\left(n\right) = \alpha v_o\left[\left(n-1\right)T_s\right] + g v_{in}(n-1)\left(1 - e^{-T_s/2\tau}\right) + SR \cdot t_1 e^{-T_s/2\tau}\delta(\mathrm{n})$$
$$\overset{Z}{\leftrightarrow} V_o(z) = \left[g\left(1 - e^{-T_s/2\tau}\right)V_{in}(z)\,\mathrm{z}^{-1} + SR \cdot t_1 e^{-T_s/2\tau}\right]\Big/(1 - \alpha z^{-1}) \tag{28}$$

Wherein $t_1 = \ln\left[SR \cdot \tau / g v_{in}(n-1)\right]$. Taking nonlinear DCG into account, we just need to substitute g_1, α_1 of (14) (15) for g, α in last two equations. In comparison with (8), a factor $1 - e^{-Ts/2\tau}$ less than 1 is added to the integration gain in (27), however, besides that, the numerator in (28) has an additional constant, so we can't find out the system transfer function straightforward, making the SIMULINK modeling more complicated and needing MATLAB/SIMULINK programming language to tackle this problem further.

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