A 14-bit 2.5 GS/s DAC based on Multi-Clock Synchronization

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Abstract. This paper presents a 14-bit 2.5GS/s current-steering segmented DAC with a new technology of synchronization, called multi-clock synchronization, which is used to optimize the timing between the internal digital and analog domains. The quad-switch architecture is also adopted to mask the code-dependent glitches. The full-scale output current can be programmed over the 10mA to 30mA range, and the typical full-scale output current is 20mA. The device is manufactured on a standard 0.18μm CMOS process and operates from 1.8V and 3.3V supplies.

1. Introduction

Nowadays the communication applications call for high speed operation[1]. Since a digital-to-analog converter (DAC) acts as an interface between digital baseband and RF front-end, it is the first analog signal generator in a transceiver transmitting path and determines the maximal performance achievable in the whole system. High speed and high resolution DACs have become the critical components in many communication systems. Moreover, in these applications, dynamic performance of the DAC, such as SFDR, IMD, are more important and concerned than its static performance such as integral nonlinearity (INL) and differential nonlinearity (DNL)[2]. Nevertheless, sampling frequency, linearity, and resolution are tradeoffs that should be carefully taken into account. The reported problems in achieving high update rate in companion with good linearity up to Nyquist frequency highlight the necessary of synchronization of the data and clock[3] .For those high-speed applications, current-steering DACs are usually considered as an appropriate architecture[4]. And recently published high-speed converters have provided the update rate up to GS/s[5,6].

In this work, a novel DAC based on multi-clock synchronization is presented. This paper firstly describes the design of a 14-bit current-steering segmented DAC with an update rate of 2.5GS/s in the 0.18μm CMOS technology. Section II describes an overview of the DAC architectures and the design considerations of its major blocks, including the LVDS receiver, DAC core and the bias circuits. Section III comes up with the architecture of the multi-clock synchronization, including critical circuit such as phase detector and delay cell. The measurement results are presented in the Section IV. The conclusions are given in the Section V.

2. DAC Architecture

Fig. 1 shows the architecture of the 14 bit 2.5 GS/s DAC. The LVDS data ports receive data, along with an embedded D_CLK clock that is synchronous with the data. The data is then transferred to the data latch and the DAC core. In the transition, the D_CLK and the DACCLK is

synchronized, which means the data and the DACCLK is synchronized. The voltage VREF provides a voltage reference to the DAC BIAS to bias the current source in the DAC CORE. The DAC CORE converts the digital words to analog current, the output current flows through IOUTP/N ports to the load. The typical full-scale current output is 20mA. Since the DAC output is current, the linearity is independent of the output voltage swing, as long as the output loading performs a linear conversion and the finite output impedance is not a dominant error source.
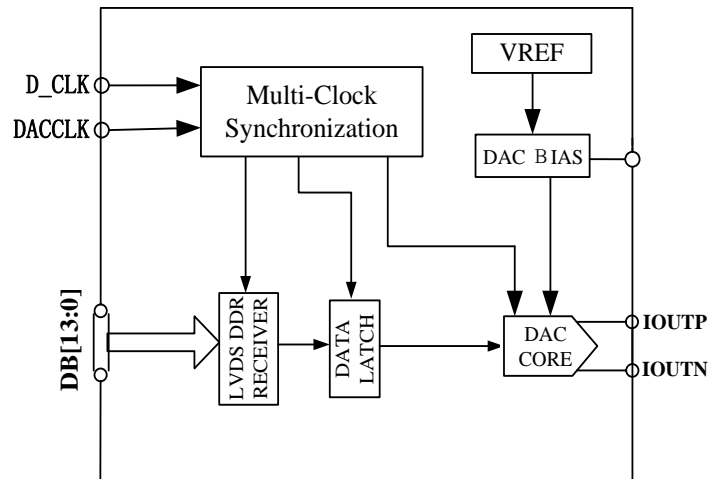

Fig. 1 DAC architecture

LVDS Receiver. The LVDS receiver receives the standard LVDS signal and converts to the CMOS signal. The interface is double data rate (DDR). Since the data rate is 1.25G bps, Multi-stage architecture is used and the data control clock is used in the comparator. The pre-amplifier, source follower and the comparator form the three-stage differential comparator. The AMP at the output amplifies the differential signals to make them rail to rail.
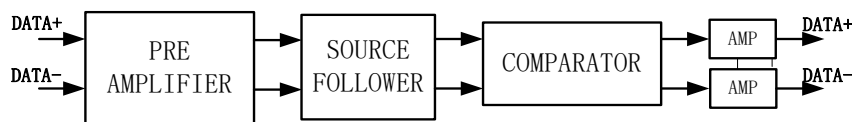

Fig. 2 LVDS receiver

DAC Core. The basic structure of this design is shown in Fig.3, which provides 14 bits of overall resolution. In this paper, the 5MSBs are thermometer-coded and the remaining 9 LSBs are binary-coded for the purpose of keeping balance of the area and the power consumption. The 5MSBs are decoded to 15 bits thermometer-code and implemented in a unary way, each unit element consists of an active cascode PMOS current source and quad-switch architecture. The full-scale output current is the major portion of the current in the analog supply. A popular output current for previous designs was 20mA because it provided 1V signal swings through 50Ω resistor.
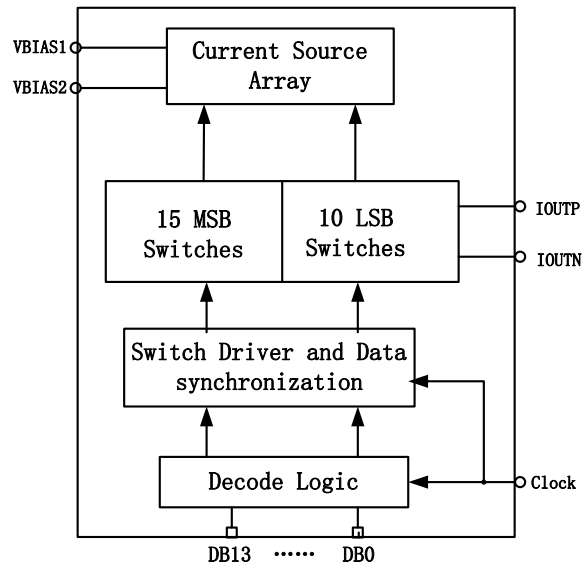
Fig. 3 Block diagram of DAC core

The Bias Circuit of DAC Core. The bias circuit biases the current source and the cascode PMOS in the current source array. Since the bias voltage directly affects the output current's linearity, the bias voltage should be carefully designed. In this design, the bias voltage of the current source is produced in fig.4.The bias1 connects to the current source transistor's gate, and the bias2 connects to the cascode PMOS transistor's gate. An amplifier is used to the bias circuit to form a feedback loop, making the bias1 voltage stable and enhance the output impendence of the current source.
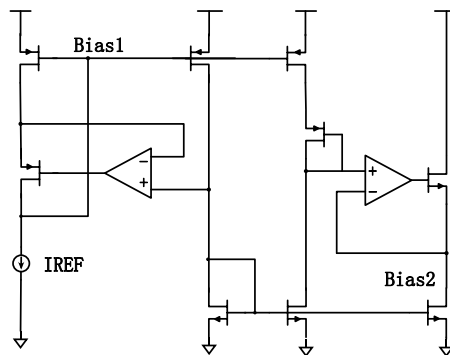
Fig. 4 Bias circuit of DAC core

3. Multi-Clock Synchronization

Since the DAC clock is 2.5GHz, slight changes in the environment (temperature, supply voltage, etc.) can induce evident noise in the clock domain. At high frequencies, clock jitter can reduce the SNR and bring mismatch in clock drivers that will result in nonlinearities. In this design these problems are solved by using multi-clock synchronization circuit to ensure that the data and the clock are synchronized.

There are three kinds of clock in the DAC, the data clock, the digital DAC clock and the analog DAC clock. The data clock is used to sample the digital input word, the digital DAC clock is used in the logic circuit such as decoder, digital control circuit and the analog DAC clock is used in the current switch array. The Multi-clock synchronization circuit makes sure that different clocks on the entire chip are synchronized. That is to say the phase relation between them must be well controlled.

Architecture. When the clock is delivered into the chip, two steps are carried out in sequence to synchronize the data and the clocks. First, the data clock and the DAC clock is synchronized, after that, the analog DAC clock and the digital DAC clock is synchronized. With the delay controller adjusting the delay of the clocks, the three clocks can be kept synchronized when noise comes up. Since the LVDS circuit use DDR mode to sample the data, the frequency of the data clock is half of the DAC clock. This makes it easier to implement the LVDS circuit and the power consumption of the synchronization circuit is reduced. The DAC clock is delivered into the circuit through the delay line controlled by the delay controller, and then the frequency is divided by 4, the phase detector compare the phase difference of the 1/2 data input clock and the 1/4 DAC clock, output the control word to control the delay controller, obtaining proper phase relationship. The analog DAC clock and the digital DAC clock are synchronized in the same way, except that there is no frequency divider in the second synchronization circuit. The block diagram is shown in Figure 5.

Fig. 5 Block diagram of multi-clock synchronization circuit

Phase Detector. The phase detector is shown in Fig. 6. It detects the phase differences between the two clocks in and then output the phase relationship of the two clocks. A high speed comparator is used as the phase detector in the first part of the synchronization circuit. The frequency divider divided the DAC clock by 4 and output four clocks to the phase detector. The four clocks are of the same frequency and delayed 1/4 period one by one. When the data input clock and 1/4 DAC CLK are high, the output of the phase detector is 0. With four clocks compared with the data input clock in four phase detectors, there will be four states in the output. According to the state of the phase detector, the delay controller controls the delay line to adjust the phase relationship of the two clocks domain.

Fig. 6 Clock phase detector

Delay Cell. The schematic of the delay cell is shown in Figure 7 and the connection of delay cells are shown in Figure 8.Since the frequency is as high as 2.5G Hz, the CML logic cell is used as the delay cell in the controller delay line. The delay of one cell is 20ps, and the period of the DAC clock is 400ps, which means the number of the delay cells is 20 at least.
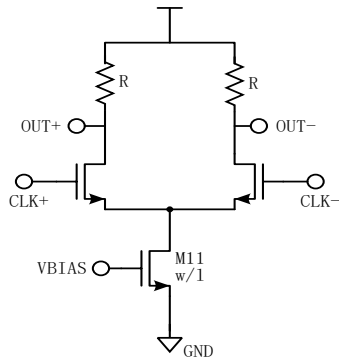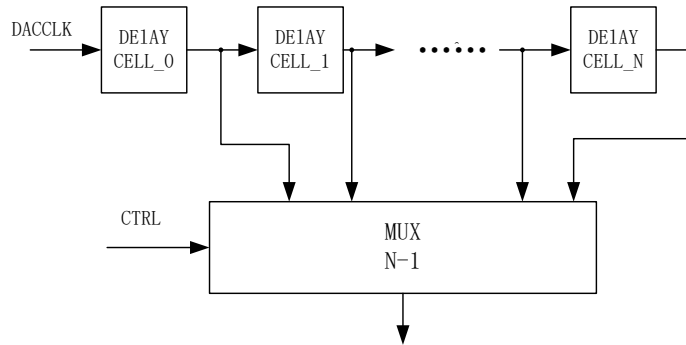

Fig. 7 Delay cell

Fig. 8 Delay line

4. Measurement Results

The DAC is fabricated in a 0.18 um CMOS process with 1.8/3.3V power supply. The DNL and INL characteristics of the proposed14-bit DAC with 20mA output current are shown in Fig.9.The DNL errors are less than ±2LSB and INL errors are less than ±3LSB.
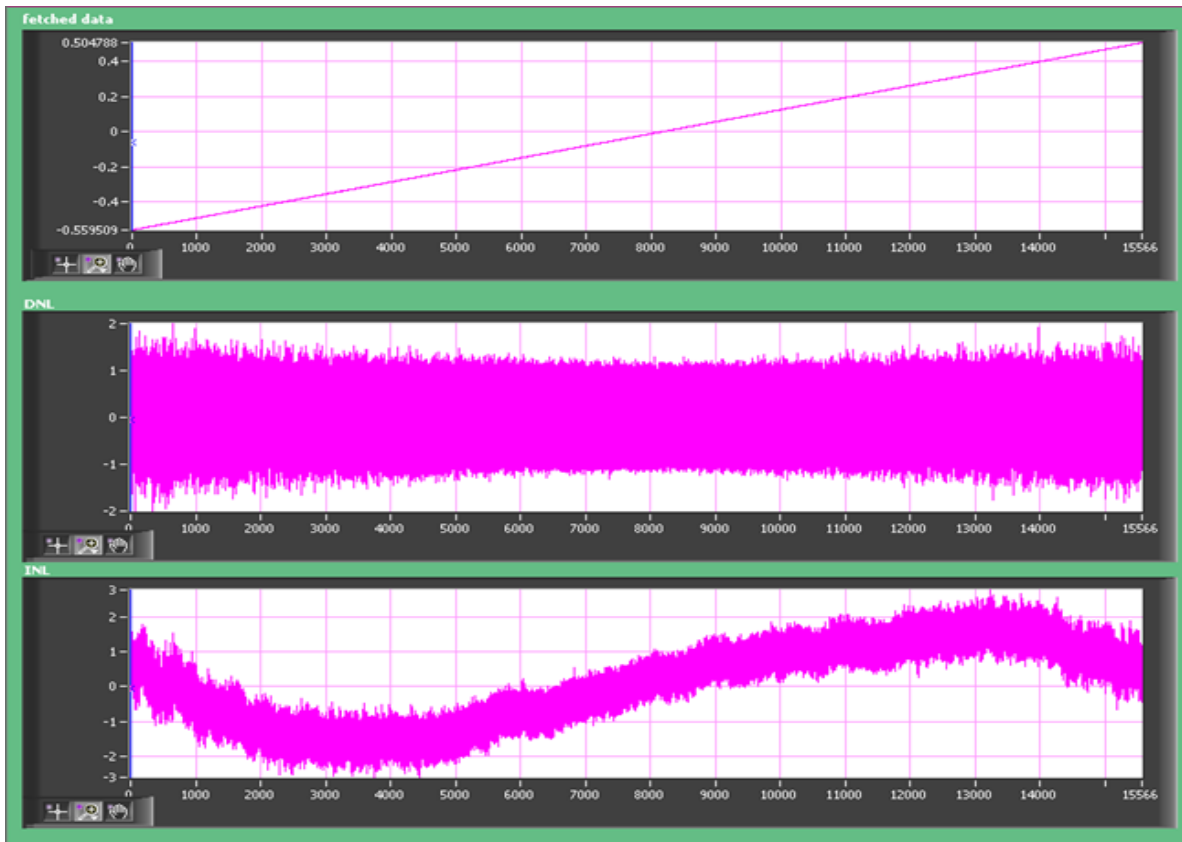

Fig.9 DNL and INL of the DAC

The dynamic test is based on an auto-analyzing system. The DAC is tested with a 100MHz input signal at 2.5GS/s sampling rate, the measured SFDR is 67dBc and IMD is 90dBc. The measured performance of the DAC is summarized in table.1.

Table 1 Measured performance of 14-bit 2.5GS/s DAC

Process	0.18μm CMOS
Resolution	14 bit
Sampling Rate	2.5[GS/s]
Power supply	1.8/3.3[V]
Full-scale output current	20[mA]
DNL/INL	±2/±3[LSB]
SFDR(100MHz @ 2.5GS/s)	67[dBc]
IMD(100MHz @ 2.5GS/s)	90[dBc]

5. Conclusion

In this paper, a novel DAC based on Multi-clock synchronization is presented for communication applications. According to the measurement results, the SFDR is 67dBc for 100MHz @ 2.5GS/s, and the IMD is 90dBc for 100MHz @ 2.5GS/s. The DNL and INL range are ±2LSB and ±3LSB respectively with 20mA output current.

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