Analog Front-end Design of Passive RFID Tags for ISO/IEC 14443 and 15693

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Abstract. This paper presents a design of analog front-end of passive RFID tags for ISO/IEC 14443 and 15693 by using SMIC 0.18μm 2P4M CMOS process. In order to have better performance, three rectifiers have been designed and compared, LDO and low-pass filter have been designed to obtain a high PSRR and a large range of subcarrier frequency respectively. As the post-layout simulation results showing, this design can satisfy both the ISO/IEC 14443 and 15693, and be adopted in many applications.

Introduction

The high frequency radio frequency Identification (HF RFID) protocols of ISO/IEC 14443 and 15693 are widely used in China. The access distance definition of ISO 14443, which are used in identity card, passport, union pay card and bus card with encryption, is 7cm - 15cm. However, the access distance of ISO 15693, which are used in security, access control without encryption [1-2], is around 1m. The comparison of ISO/IEC 14443 and 15693 is shown in table 1. In this paper, a analog front-end of HF RFID tags are designed for those two protocols, which enables a single tag for different applications.

Table 1 Comparison of ISO/IEC 14443 and ISO/IEC 15693

Protocol	Operating Field Hmin [W/m]	Operating Field Hmax [W/m]	Carrier for 100%ASK [μs]	Carrier for 10%ASK [μs]	Data rates [Kbits/s]
ISO/IEC 14443	1.5	7	2~4.5	4	106
ISO/IEC 15693	0.15	5	6~9.44	6~9.44	26.48

Previously, there are some papers which are trying to optimize the front-end blocks of tags. A cap-less ASK demodulator was designed to save the chip area [3]. Another ASK demodulator which can handle up to 2Mbps with a carrier frequency 13.56MHz was reported [4]. A 4xVDD rectifier is capable of receiving 14 V ASK modulated signal with the cascoded diode-connected NMOS transistors [5]. LDO is another key block in addition to demodulator. A regulator was presented which can provide 2 mW power, with -38.7dBm backscatter power levels [6]. All of those make it possible to design a single tag for both the two protocols.

In this paper, we present the design of the analog front-end of HF RFID tags for both ISO/IEC 14443 and 15693 using SMIC 0.18μm 2P4M CMOS process. The fron-end mainly consists of three blocks, including the demodulator, the power generator and clock generator. Forthermore, the power generator consists of four parts, they are the rectifier, lever-limiter, bandgap and the LDO.

Analog Front End of HF RFID Tags

The concerns of design are the power consumption and the robustness of demodulator. Three different rectifiers are compared to improve energy conversion efficiency. The high PSRR of LDO is obtained to suppress the power noise. Furthermore, the demodulator is optimized to handle different subcarrier frequencies of ISO/IEC 14443 and 15693. Fig. 1 shows our building blocks of analog circuit.

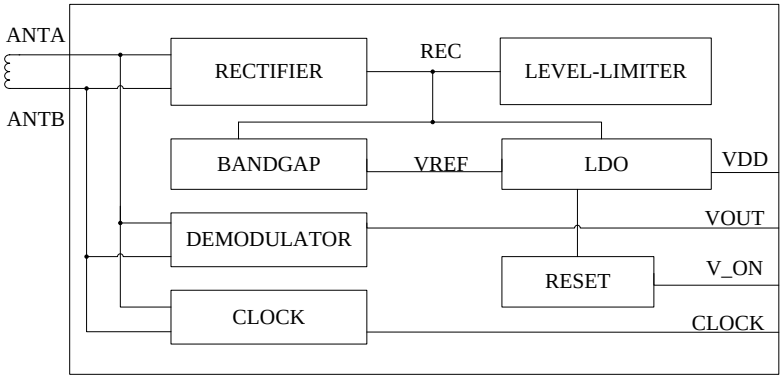

Fig. 1 The building blocks of analog circuit

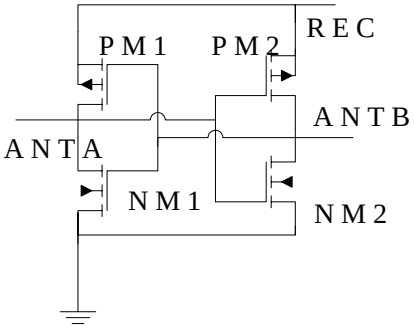

Fig. 2 Gate cross-connected rectifier

A. Rectifier

Rectifier is one of key blocks of high-frequency radio-frequency identification tags, and it directly determines the RFID Tag's communication distance. Three rectifiers popularly used in the design of RFID Tags have been selected and compared, including MOSFET full-wave rectifier [7], half gate cross-connected rectifier [6], and gate cross-connected rectifier [8]. In the Fig.ure 2, V_{thn} represents the threshold voltage of PM1 and PM2, and V_{REC} is the output voltage of the rectifier. In the positive period, the current flows from terminal ANTA to PM1, and goes through the RC load circuits to the ground when the node voltage V_{ANTA} is higher than V_{REC} and V_{ANTB} is lower than $V_{REC} + V_{thn}$. The gate cross-connected rectifier has the lowest turn-on voltage, as shown in table 2.

Table 2 The comparison of turn-on voltage of rectifiers

	MOSFET full-wave	half gate cross-connected	gate cross-connected
Turn-on Voltage	$V_{REC} + V_{thn}$	$V_{REC} + V_{thn}$	V_{REC}

B. Bandgap and LDO

LDO provides power supply voltage (1.8 V) to make all circuits work well. The stability of LDO needs to be pay more attention under the changing V_{REC}, which means a high PSRR is desired in this design.

Fig. 3 (a) shows the details of LDO. PM2 has a quite large W/L ratio to ensure the current of 10 mA. Vref generated in the bandgap is compared with the gate voltage of PM3 to generate the error signal, which is connected to the gate of PM2. High gain of the EA and a accurate Vref are desired to the requirement of the LDO PSRR [9].

Fig. 3 (b) shows the circuit of bandgap. It is composed of Q0, Q1, R1, R2 and R3. The reference voltage Vref is generated by using the error amplifier and the current mirror. The output of the EA is connnected to PM4 and PM5. The effects from the noise of Vrec and varying temperature is mitigated

by the feedback loop. Q0 is 24 parallel connected PNP BJT while Q1 is only 1 PNP BJT. Here, Vref can be calculated by

$$Vref = V_t \frac{R2}{R3} \ln 24 + V_{eb1} \quad (1)$$

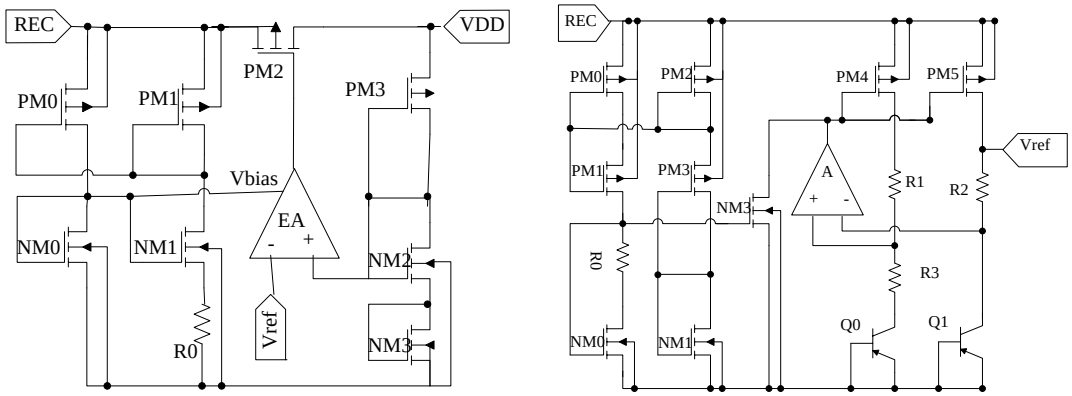

Fig. 3 (a) LDO (b) Bandgap

C. Demodulator

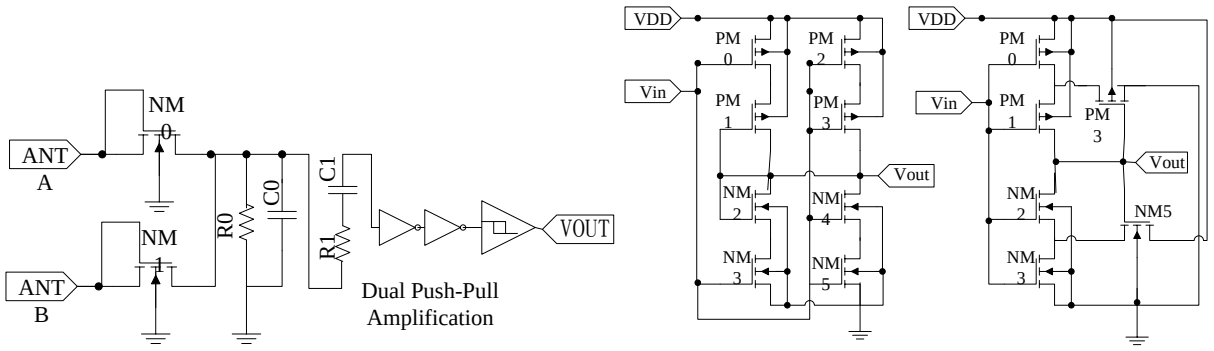

Fig. 4 (a) Demodulator (b) Push-pull Amplifier (c) Schmitt Trigger

A low-pass filter (R0-C0) is used to recover the subcarrier from the carrier. According to the table 1, the subcarrier frequency is from 106 KHz to 250 KHz. Therefore, the cut-off frequency of the filter is set to 500 KHz. The high-pass filter consisting of R1 and C1 is used to extract the jumping edge of subcarrier. The jumping edge is then amplified by dual push-pull amplifer, which is showed in Fig. 4 (b). Schmitt trigger shown in Fig. 4 (c) recovers the codes from the amplifier's output.

D. Clock

The clock (13.56 MHz) of a passive tag should be extracted from the carrier, and then be divided to be the main clock of the digital circuit. As shown in Fig. 5, the cross latch is composed of PM2, NM2, PM3 and NM3, which forms a positive feedback. In order to sustain higher breakdown voltage, 3.3V NMOS transistors are used as the input NMOS transistors（NM0 and NM1）. Besides, NM0 and PM3 also acts as a common-source amplifier when V_{ANTA} is higher than $V_{th, NM0}$.

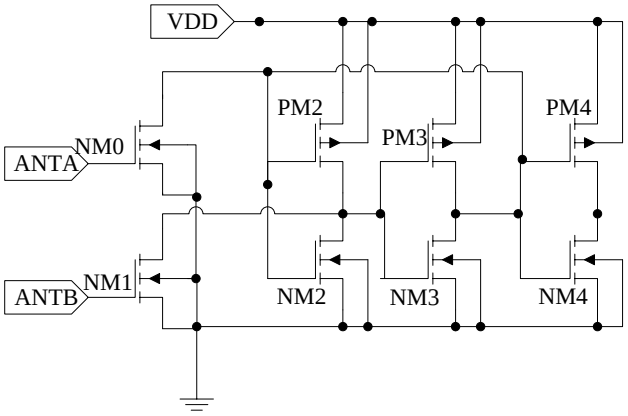

Fig. 5 Clock

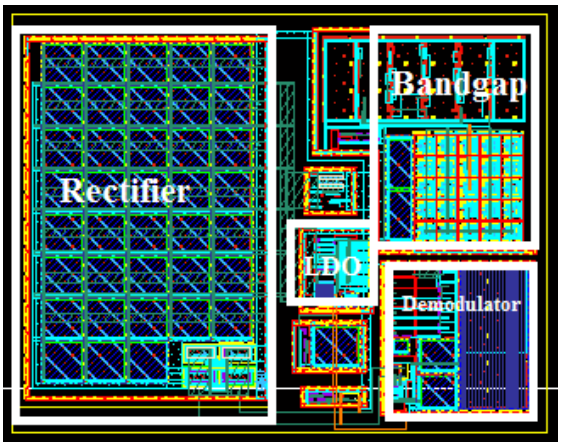

Fig. 6 Layout of the front-end of HF RFID tags

Layout and the post-layout simulation

Fig. 6 shows the layout of the front-end of HF RFID tag using SMIC 0.18 μm 2P4M COMS process. The layout size is around 365μm×285μm.

The modulation mode of 10% ASK is taken, and the operating field has been scanned from 0.15A/m to 7A/m. The results shows that V_{REC} varys from 2.5V to 4V. The level-limiter will be turned on once V_{REC} is higher than 4V. The output voltage of bandgap Vref is 1.1 V, and the ripple voltage is less than 2%. The output of LDO is 1.83V, and its ripple is around 5%. The different data rate of 53 Kbps, 106 Kbps, 212 Kbps and 424 Kbps have been also simulated. Fig. 7 give the results under 1.5 A/m operating field.

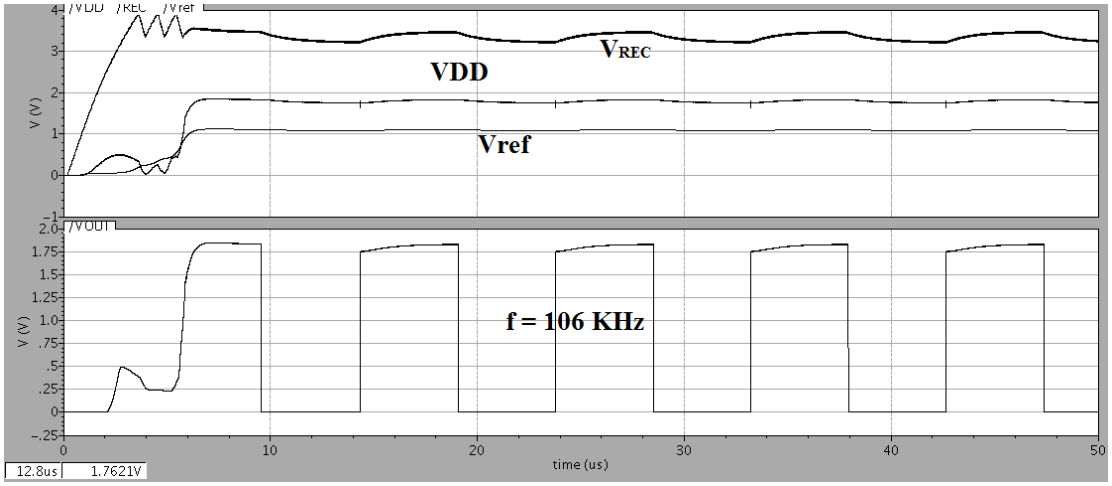

Fig. 7 Simulation results of analog front-end

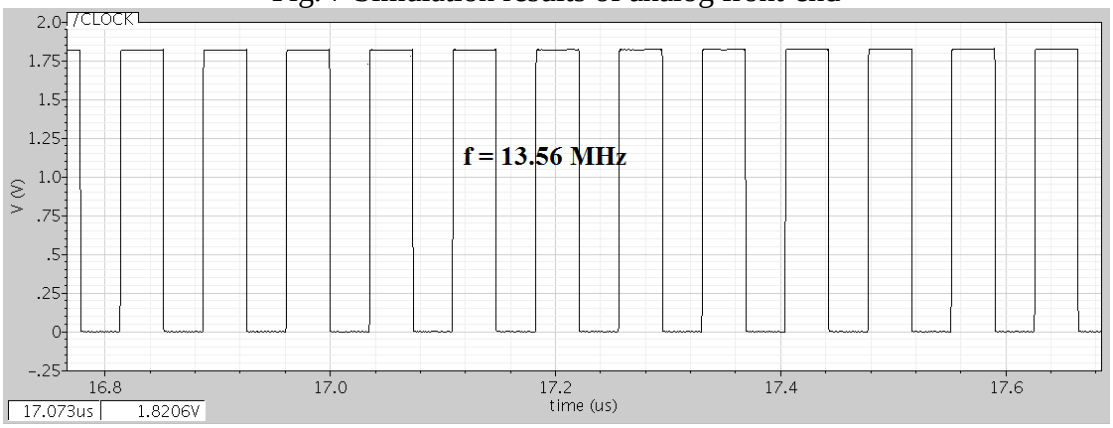

Fig. 8 Clock simulation results of analog front-end

Fig. 8 shows the clock simulation result. The period of the clock is 74 ns under 1.5 A/m operating field, satisfying the requirement of ISO/IEC 14443 and 15693, namely 13.56MHz ±7kHz.

Conclusion

The front-end of HF passive RFID tag IC in conformance with the ISO/IEC 14443 and 15693 has been presented in this paper. The tag IC which is designed using the 0.18 μm 2P4M COMS process achieves large range of subcarrier frequency and operating field. The post-layout simulation shows that our HF RFID tag satisfys both ISO/IEC 14443 and 15693, and can be adopted in many applications.

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