A chopped charge pump of PLL

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Abstract. In this paper, a chopped charge pump with matching up and down pulses was introduced. The proposed topology is based on differential current sources and sinks. a switching circuit for switching on in a first phase one current source of each pair to provide up current pulses, and switching on in a second phase the other current source of each pair to provide up current pulses. The chopped charge pump can eliminate static phase error of PLL. The proposed PLL circuit is designed based on the 0.18um CMOS process with a 3.3V&1.8V supply voltage.

Introduction

IN recent years, digital frequency synthesizers have become very popular thanks to the flexibility offered by digital signal processing. Digital communication system are shown in figure 1.Performances equivalent to analog solutions have been combined with the possibility of exploiting efficient digital calibrations and fast frequency-phase locking acquisitions [1].

The common design practice for systems with low-noise input clock is to critically damp or over damp a PLL to minimize peaking in jitter transfer function and to design the loop with the highest possible bandwidth to eliminate the effects of noise sources at the output. Very low bandwidth and high damping factor are commonly used to filter a noisy input clock with a clean oscillator within the PLL. By understanding the sensitivity of jitter to loop parameters, we can refine these common practices in designing low-jitter PLLs. Section II introduce basic structure of PLLs, It will start with an introduction of the loop as a feedback control problem, with both the similarities and differences to traditional control problems. In Section III, chopped charge pump was introduced which provides matched up and down output current pulses. So improved PLL works well with zero static phase offset. In Section IV, the simulation results of the improved PLL are reported.

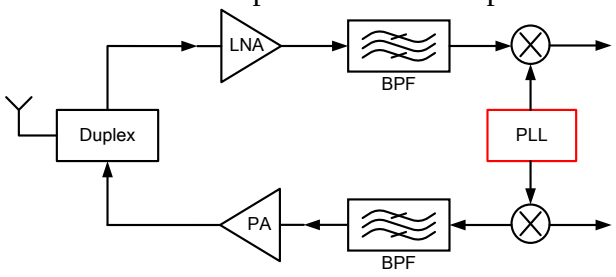

Fig. 1 A general DSP communication system

PLL Basics.

The basic idea of a phase-locked loop is that if one injects a sinusoidal signal into the reference input, the internal oscillator in the loop will lock to the reference sinusoid in such a way that the frequency and phase differences between the reference sinusoid and the internal sinusoid will be driven to some constant value or 0 (depending on the system type). The internal sinusoid then represents a filtered or smoothed version of the reference sinusoid. For digital signals, Walsh functions replace sinusoids.

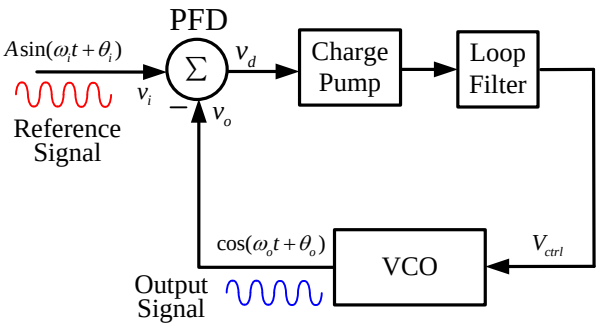

Fig. 2 A classic mixing phase-locked loop

Typical block diagrams of PLLs in the literature resemble Figure 2, in which a high frequency low pass filter is used to attenuate the double frequency term and a band-pass filter is used to limit the bandwidth of input signals to the loop. A general sinusoidal signal at the reference input of a PLL as shown in Figure 2 can be written as:

$$v_i = R_1(t) = A\sin(\omega_i t+\theta_i) \tag{1}$$

Without loss of generality, we can assume that the output signal from the Voltage Controlled Oscillator (VCO) into the PFD is given by

$$v_o = VCO_{out}(t) = \cos(\omega_o t+\theta_o) \tag{2}$$

Typically, analysis of such a PLL is done by taking several simplifying steps. Using the familiar trigonometric identity in terms of the PLL and then making two fundamental assumptions leads to the commonly used model of the analog PLL[2,3]. Making these assumptions leads to the PLL model shown in Figure 3.

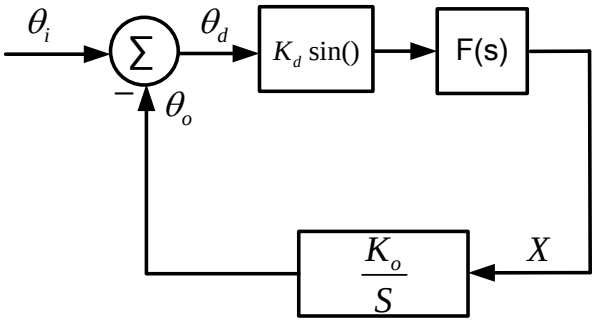

Fig. 3 Conceptual block diagram of PLL

A conventional tri-state PFD includes a pair of bi-stable devices(eg., D-type flip-flops) and gating logic. Because there is mismatch in the clock-to-Q delay in flip-flops as well as mismatch in the reset-to-Q delay. the up and down pulses have slightly mismatched pulse widths which leads to output offset error. Moreover, any mismatch in the propagation delays of the gating logic in the up and down paths between the PFD and the charge pump will cause an output offset which results in static phase error.

The current sources of the single-ended charge pump of conventional dual bandwidth PLL synthesizers typically utilize different types of devices for the pump up and pump down current sources in the charge pump ,e.g., a PMOS device for up current pulses and an NMOS device for down current. Typically, the matching between the currents from the two different devices is no better than five percent. The result is mismatched up and down current pulse magnitudes, that the charge pump generates. The PLL structure that is commonly used in conventional synthesizers is a closed loop feedback system with two integrators in the forward path.

Hence the PLL synthesizer will reach equilibrium with whatever static phase error the PLL synthesizer needs between the PFD inputs to ensure DC balance at the loop filter node connected to the charge pump output[4]. The DC or average value of the static phase error will be the amount required to cancel out the excess charge delivered to the loop filter due to the mismatch. For example, a

mismatch of 5%with a 3 ns minimum PFD turn-on time would result in a phase skew of about 150ps between the PFD inputs. In this example, if the RF output frequency is about 1850MHz,a phase skew of 150ps would corresponds to a static phase error of 1000 at the output. Similarly, other imperfections in the PFD and/or the conventional single-ended charge pump, such as charge injection in the charge pump switches and leakage current at the output, will result in static phase error at the output of the PLL.

Modified Charge Pump

PLL synthesizer typically includes phase frequency detector(PFD) responsive to a reference frequency signal.PFD generates up and down pulses which have mismatched pulse widths that result in output phase offset and charge pump generates up and down output current pulses with mismatched magnitudes that also result in output phase offset, then static phase error must exist.

Chopped charge pump of this paper includes first pair of current sources that source current out on CPO- to loop filter; second pair of current sources, that sink current in CPO+ to loop filter. The pump up operation increases the differential voltage between CPO- and CPO+ .Hence, up current is sourced out through CPO+ and sink into CPO- .

Switching circuit switches on in a first phase, $\Phi 1$,one current source of first pair of current sources and second pair of current sources, e.g., current source and current source to provide up current pulses on CPO+ and the other current source of PMOS array to provide current down pulses on CPO-.Then, in a second phase, $\Phi 2$, switching circuit switches on the other current source of pairs provide up and down current pulses.

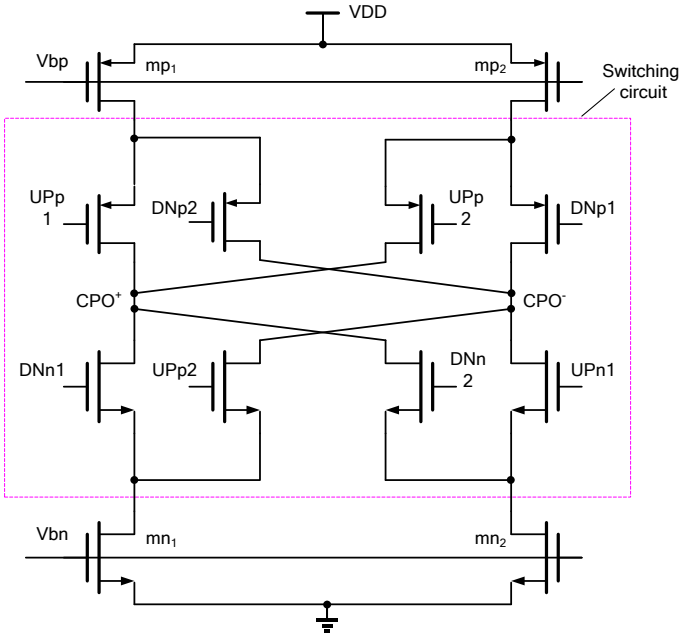

Fig. 4 Modified current switch

By selectively alternating the up and down current sources which provide the up current and down current pulses matched current up and current down pulses are generated by chopped charge pump over two phases which eliminates the corresponding need for compensating static phase offset in the PLL.

As discussed above, differential charge pump utilizes a pair of PMOS and NMOS transistor to generate up current Pulses and another pair of PMOS and NMOS transistor to generate down current pulses. The up versus down mismatch problem is now significantly reduced because it depends on how a PMOS transistor matches a PMOS device and NMOS transistor matches a NMOS device. Utilizing a fully differential architecture of differential charge pump with identical up and down current sources reduces the mismatch by at least an order of magnitude when compared to conventional single-ended

charge pump. The addition of the chopping technique as described above to the differential structure of differential charge pump eliminates any residual mismatch that may still exist between the two identical halves of differential charge pump due to process variations.

Layout and Conclusion

To verify the effectiveness of this chopped charge pump, a LC tank PLL was constructed in 0.18um CMOS process technology. The PLL utilizes differential PFD and Loop filter.

Top metal layer was used to help improve the VCO inductor Quality. Excellent on chip inductor dramatically reduces 1/f noise.Charge pump layout was shown in figure 5.

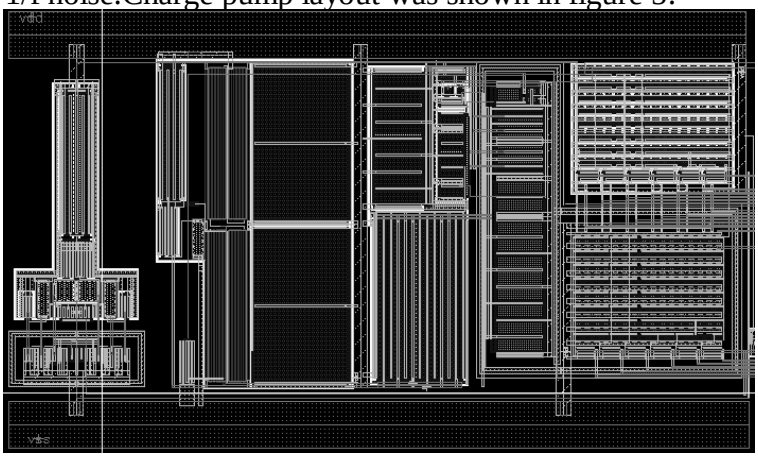

Fig. 5 Chopped charge pump layout

In terms of PLL, a new chopped charge pump was presented which helps to reduce static phase error.

This paper introduces chopped charge pump. Basic knowledge of PLL was given in section II. In order to verify the chopped charge pump, A LC thank was constructed with 0.18um CMOS process. The PLL can handle reference signal until 125MHz,Simulation shows chopped can dramatically reduce static phase offset.

References

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