A New High Speed LVDS Repeater

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Abstract. A LVDS receiver and driver for LVDS repeater are introduced, which can buffer LVDS one channel to four. As a result, the repeater can speeds up to 633Mbps.It is useful in long distance transmission to reduce signal attenuation.

Introduction

Low-voltage differential signal (LVDS) technology was originally developed in order to provide a low-power and low-voltage alternative, to other high-speed I/O interfaces for point-to-point transmission, such as emitter-coupled logic (ECL). As the performances of A/D converter and other systems such as SOC have improved in recent years, the requirements for interface circuits are becoming much higher. But the signal will be attenuated very badly when transmitted in long distance. It influences the receive terminal seriously.

This paper describes the design of a new high speed LVDS repeater developed in standard 0.6um CMOS process technology ,which can speeds to transmit data at speeds up to 655 Mbps at relatively long distances. In that way we can get better signal .

Structure

As shown in figure 1, the proposed LVDS repeater is mainly consists of one LVDS receiver and four LVDS drivers. The output of the receiver connects the four LVDS driver. It buffers LVDS one channel to four. IN+ and IN- are positive port and negative port respectively of the LVDS input. A1~A4 and B1~B4 is the positive port and negative port respectively of the LVDS output.

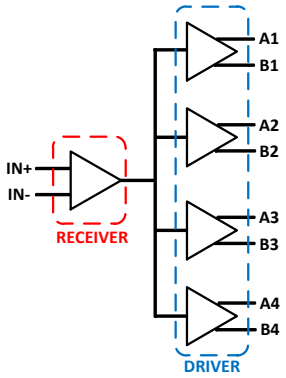

Figure1. Functional Block Diagram

A. Receiver

Receiver is the most important part of the whole design, and it converts LVDS signal to LVCOMS signal for the LVDS drivers. Figure 2 shows the block diagram of the receiver .The complementary inputs are adopted to support the wide common mode voltage input. The second stage is current selection block, they select the better current signal and put them on the diode MOSFET N8 and N9.The third stage is a comparator.

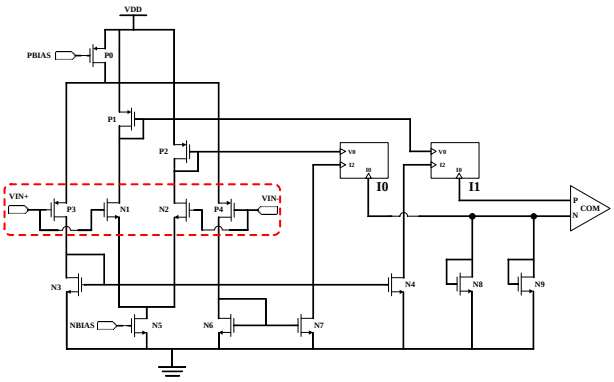

Figure 2. Receiver

Considering the wide common mode voltage input, we introduce the complementary input stage. As the red dotted frame shows, N1、N2、P3、P4 are the differential inputs. When the input common mode voltage is wide enough, the complementary inputs work in turn. When the input common mode voltage is very high, N1 and N2 work and at the same time P3 and P3 are turned off. When the input common mode voltage is low enough, the situation is opposite.P1 P2 N3 N6 is the load of the input, they copy the signal with current form to the current selection block I0 and I1.

B. Max current selection block

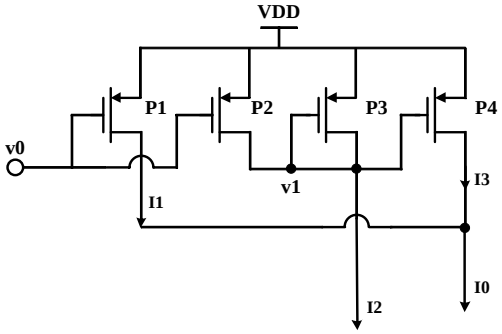

Figure 3. Current Selection Block

The signal quality of receiver is the most important in the LVDS repeater. If the output of receiver is bad, the output signal quality of the repeater is not good. In the design we propose a current selection block. Since we design the pre-receiver in order to make the input common voltage above the VTH of NMOS. At that time the current of NMOS is larger than the PMOS. When the input common voltage is below the VTH of NMOS, they are turned off , and the PMOS start work. So if we select the larger current, the comparator can get the better signal and in that way we can enhance the reliability of the design.

In the proposed current selection block we introduce four PMOS P1~P4 with the same dimension. When I2>I1， the current mirror copies the I_D of P1 to P2, so the I_D of P2 equals I1. So the I_{D_P3}=I2-I1. And V_{SG_P4}= V_{SG_P3}， then I_{D_P4}=I3= I_{D_P3}=(I2-I1). At last I0=(I1+I3)=I1+(I2-I1)=I2,and they select the larger current I2.

When I1>I2, Since I2 is limited by the tale current source, and the circuit can raise v1 to make the I_{D_P2}=I2. And the raised v1 make P3 cutoff and I3=0. At last I0=I1+I3=I1+0=I1.

From the simulation above we can get the branch with larger current. The current signal forms voltage signal via N8 and N9. In that way the comparator get the better signal quality.

C. Comparator

In practice application, circuits always work with noise. If the comparator is fast enough and the amplitude of noise is large enough too, the noise may cause transition error when the input works nearby the threshold of the comparator. So we introduce the hysteresis. As the figure 4 shows, we design a OTA comparator which has two stage. The first stage consists of P0~P2、N0~N3,and N2、N3 introduce positive feedback and hysteresis .When VIN+ is larger enough than VIN- , P1、N1、N2 turn on, P2、N0、N3 turn off, the current mainly flows into P1 and N2. the second is the common source amplifier.

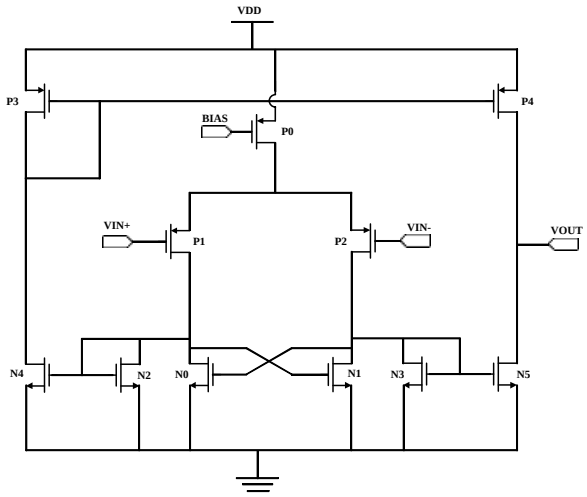

Figure 4. The Comparator

With the increasing of VIN+, current flowing into P2 increases gradually and so as the current flows into N1 until it equals current flows into N0. Assume that the tale current source is I_{SS}, then the current flows into the differential input is :

$$I_{P1}=I_{N0};\ I_{P2}=I_{N1};\ I_{SS}=I_{P1}+I_{P2} \tag{1}$$

Since $V_{GSP1}=\sqrt{\frac{2I_{P1}}{\beta_{P1}}}+V_{THP1}$; $V_{GSP2}=\sqrt{\frac{2I_{P2}}{\beta_{P2}}}+V_{THP2}$ (2)

So the negative hysteresis voltage is :(assume that $\beta_{P1}=\beta_{P1}=\beta_A$,$\beta_{N0}=\beta_{N1}=\beta_B$, $\beta_{N2}=\beta_{N3}=\beta_C$)

$$V_{SPL}=V_{GSP1}-V_{GSP2}=\sqrt{\frac{2}{\beta_A}}(\sqrt{I_{P1}}-\sqrt{I_{P2}})=\frac{\sqrt{I_{SS}}}{\beta_A}(\frac{\sqrt{\beta_C}-\sqrt{\beta_B}}{\sqrt{\beta_C}+\sqrt{\beta_B}}) \tag{3}$$

Similarly, we can get the positive hysteresis voltage is :

$$V_{SPH}=\frac{\sqrt{I_{SS}}}{\beta_A}(\frac{\sqrt{\beta_B}-\sqrt{\beta_C}}{\sqrt{\beta_C}+\sqrt{\beta_B}}) \tag{4}$$

Through the above calculation ,we can get the hysteresis via adjusting the dimension of the first stage. Usually the voltage is 25mV~30mV.

D. Driver

The LVDS Driver adopts the traditional structure with common mode feedback. It get the common mode voltage .Comparing the VREF, the output of CMFB adjust the current source .The current flow direction is shown in Figure X. In1 and In2(IN1- and IN+ are the opposite logic signal) .When IN1 is low(IN2 is high simultaneously),P1 and N2 is turned on and P2 \N1 is turned off. The current flows from P1-Rload-N2 and form the +350mV LVDS(as the red arrow shows)。 On the contrary, when IN2 is low(IN1 is high simultaneously),P2 and N1 is turned on and P1、N2 is turned off. The current flows from P2-Rload-N1 and form the -350mV LVDS(as the blue arrow shows). In conclusion, the opposite current IS forms the '1' and '0' logic LVDS when it flows pass RLOAD.

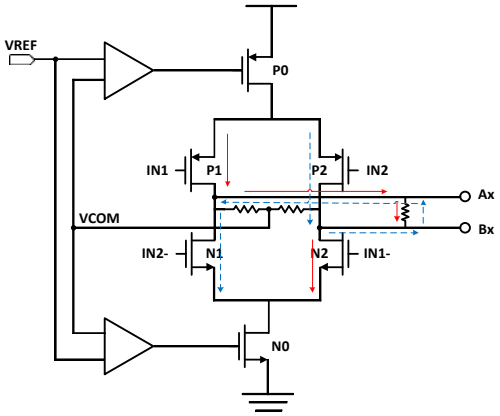

Figure 5. The LVDS driver

E. Simulution and layout

The proposed circuit was simulated with the parasitic as shown in figure 5 and figure 6. The output drives a 100 Ω resistor and two capacitor load which is 10pF.

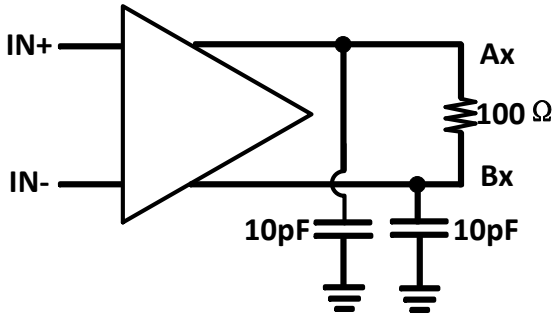

Figure 6. Simulation Model

Figure 7 shows the waveforms of the receiver that the common mode voltage of input varies as a sinusoidal vaveform at frequency of 1MHz and the input differential signal is at 50MHz with 200mV differential voltage. The result shows the receiver works at the common mode voltage between 0V to 2.78V(the power is 3.3V).

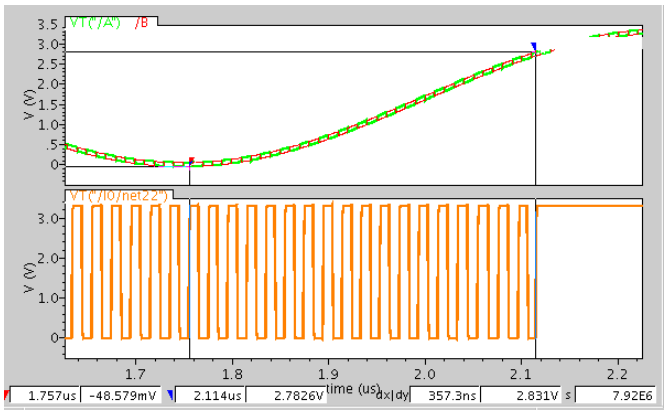

Figure 7. Input and output of receiver with wide common mode voltage input

Figure 8 and figure 9 shows the waveform of the repeater at frequency 50MHz(left) and 400MHz(right).It proves that the design can work at the data rate of 655Mbps and Table I shows the performance parameters such as the delay, power consumption in different temperature. Figure 10 shows the layout of the design and the location of the receiver and drivers.

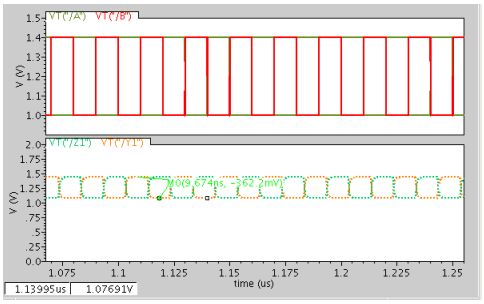

Figure 8. Waveform of the input and output(input at frequency 50MHz)

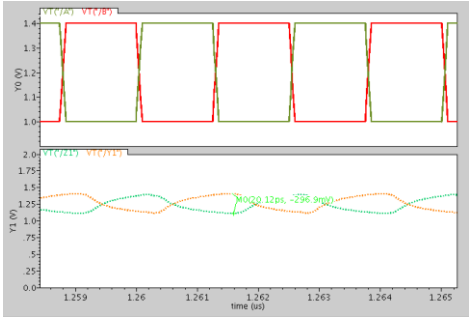

Figure 9. Waveform of the input and output(input at frequency 400MHz)

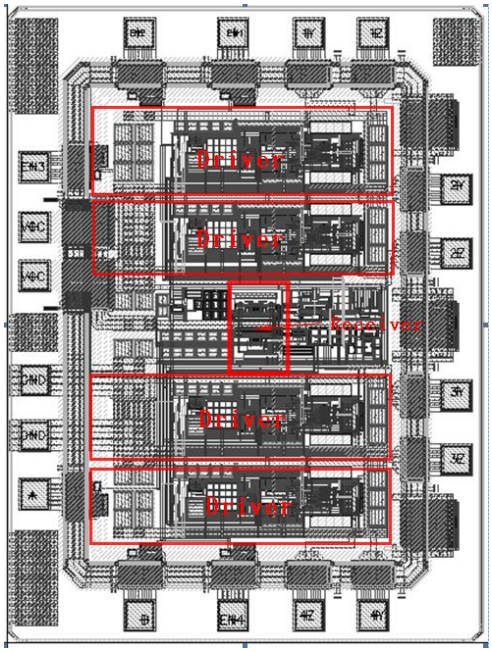

Figure 10. Layout of the repeater

Table I . Performance Parameters

	Temperature		
Parameters	-40 ℃	35 ℃	85 ℃
Propagation Delay	2.71ns	3.21ns	3.88ns
Power Current	30.9mA	30.7mA	31.5mA
Area	1690 μ m*2260 μ m		

Conclusion

The LVDS repeater was proposed in 0.6um CMOS technology. The circuit uses the technique of current selection and complementary input to get the better reliability. And it adopts the CMFB to make the common mode voltage stable. The design was simulated and verified at typical, slow and fast corner from temperature -40° C to 85° C.And it was verified that it can work under the data rate of 655Mbps . The design can be well applied in the long distance data transmission.

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