Thermal Management of The Die Bonding Architecture in 3D-ICs

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Abstract. This paper presents the thermal impact of different bonding architectures in the 3D stacked chip.ANSYS® Workbench™ 14.0 was used to model the architecture and meshed analysis was conducted. Bonding architectures that evaluated were face-to-face, face-to-back and back-to-back while all the parameters and boundary conditions were held constant. A futher discussion is the effect of changing the corresponding parameters or the boundary conditions in the thermal management performance. In that light, a list of cases consisting of increasing the heat transfer co-efficient on top of the package, improving the thermal conductivity of the bonding-layer, the TIM and the package as well as the using of microchannels were evaluated. Simulation results shows that the different bonding architecture has little impact on the maximum temperature of 3D stacked chip that without microchannels. When the microchannels are introduced, the bonding architecture has the important impact. Moreover, from the point of the thermal management performance, it found that changing only one single parameter can decrease little the maximum temperature. The case of intruducing microchannels offered significant improvement in thermal performance.

Introduction

3D integrated circuit(3D-IC) technology is an emerging technology for the near future and has received tremendous attention in the semiconductor community. As the convergence of computing and communications dictates building up rather than out. Consumers demand more functions in their hand-held devices, the need for more memory in a limited space is increasing, and integrating various functions into the same package is becoming more crucial. Over the past few years, die stacking has emerged as a powerful tool for satisfying these challenging integrated circuit packaging requirements [1,2,3].

By expanding the design space into the third dimension, 3D-IC significantly reduces average wire length, wire delay, power consumption and footprint [4-6]. Although electrical benefits are proved to have great improvements in stacked IC packages, stacking of multiple circuit layers makes effective cooling more challenging due to higher power density and larger junction-to-ambient thermal resistance. The problems of heat dissipations are more serious and catching lots of attentions than those in traditional single IC package. Hence, the thermal management of die stacking architecture becoming major concerns [7,8,9,10]. Therefore, this paper presents the thermal impact of different bonding architectures in the 3D stacked chip.

The rest of this paper is organized as follows. In the section 2, the thermal model for the three different die bonding architectures will be studied firstly and then the corresponding simulations of different cases will be discussed in the Section 3. Finally, Section 4 concludes this paper.

Thermal Modeling

In this paper, we model a die-bonding 3D integration technology that vertically stacks planar die and bonds them at the interface through bonding layer. The configuration considered here consists of two dies, where both the dies are considered as the heat sources [11].

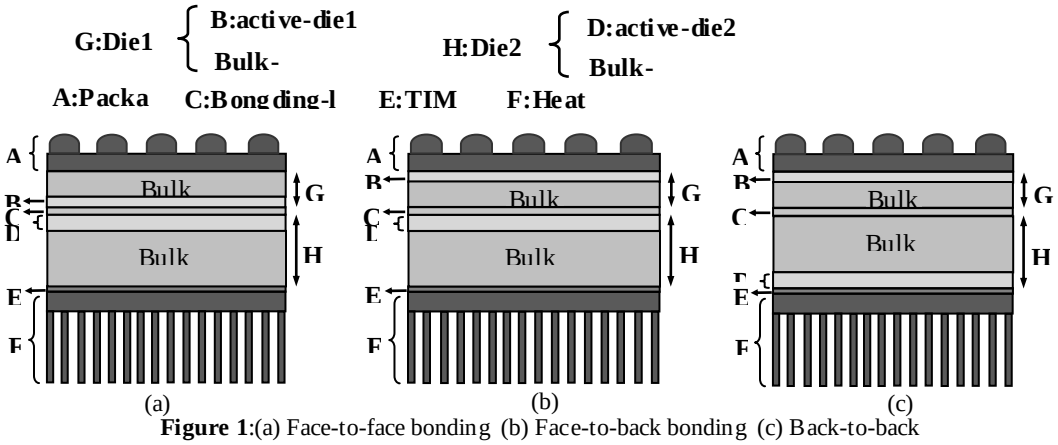


Figure 1:(a) Face-to-face bonding (b) Face-to-back bonding (c) Back-to-back

Table 1. Package Dimensions

Component	Dimension (mm^3)
Package	6.5×6.5×0.15
Bulk-1	5.5×5.5×0.4
active-die1	5.5×5.5×0.07
Bonding-layer	5.5×5.5×0.07
active-die2	5.5×5.5×0.2
Bulk-2	5.5×5.5×1
TIM-Interface	5.5×5.5×0.08
Heatsink	7.5×7.5×0.2

Fig. 1 shows three different bonding architectures that consists eight layers, Fig. 1(a) shows a 2-die 3D IC built with two planar die stacked with their active layers face-to-face(f2f) bonded by the bonding layer. Fig. 1(b) shows the face-to-back(f2b) architecture that active die2 are bonded with the bulk-1 through the bonding layer. Fig. 1(c) shows the back-to-back(b2b) architecture that die1 and die2 are stacked with their bulks bonded by the bonding layer

Table 2. Parameter settings

Parameter	Value	Unit
Material Properties		
Package	36	W/m·°C
Bulk-1	120	W/m·°C
active-die1	12	W/m·°C
Bonding-layer	0.2	W/m·°C
active-die2	9	W/m·°C
Bulk-2	120	W/m·°C
TIM-Interface	2.2	W/m·°C
Heatsink	400	W/m·°C
Boundary conditions		
Temperature-ambient	25	°C
Co-efficient(top)	5	W/m^2·°C
Co-efficient(bottom)	500	W/m^2·°C

In this paper, we simple the package as 6.5×6.5 mm^2 with the thickness of 0.15mm and the heat sink as 7.5×7.5 mm^2 with the thickness of 0.2mm. The active-die1 measures 5.5×5.5 mm^2 with a thickness of 0.07mm and has the same dimensions of the bonding layer. The active-die2 is modeled as 5.5×5.5 mm^2 with the thickness of 0.2mm. The TIM(Thermal Interface Materials)-Interface with 5.5×5.5mm^2 and 0.08 mm thick is used. Bulk-1 and Bulk-2 are the same dimensions except for the thick. Both die1 and die2 modules were stacked on the same substrate with different bonding architectures. Heat is evacuated by convection at the top and bottom ends of the stack. We assume

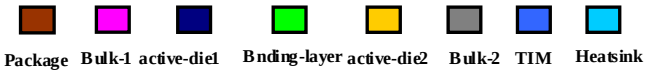
that the other parts of the body are insulated. All the parameters are listed in the Table 1. Table 2 shows the material properties of the components and the boundary conditions.

Accoding to the table 1, the corresponding bonding architecture are modeled in the Ansys workbench 14.0, as shown in the Fig. 2, Fig. 3 and Fig. 4.

Figure 2: f2f bonding architecture

Figure 3: f2b bonding architecture

Figure 4: b2b bonding architecture



For each of the bonding architecture, steady state thermal simulation was carried out as a basecase study to determine the maximum temperature using Ansys® WorkBench™ 14.0 as a Finite Element Analysis (FEA) Tool.

Basecase study further considers an application of an effective heat transfer co-efficient of 5W/m^2·℃ (natural convection) on top of the package and forced convection of 500W/m^2·℃ on bottom surface of the heatsink. The constant power levels of the active-die1 and active-die2 are assigned 1W and 2W respectively. The material properties of different layers and boundry conditions are set according to the table 2. The ambient temperature was assumed to be 25℃ .

In order to analyze the thermal impact of different bonding architecture accurately, another six different cases are presented as following:

Case 1: Increasing the thermal conductivity of the bonding-layer to 1W/m • ℃ from 0.2W/m • ℃ .

Case 2: Increasing the thermal conductivity of the TIM to 5 W/m • ℃ from 2.2W/m • ℃ .

Case 3: Increasing the effective heat transfer coefficient on top of the package to 50W/m^2 • ℃ .

Case 4: Increasing the thermal conductivity of the package from 36 W/m • ℃ to 72W/m • ℃ .

Case 5: A case that combines the case from case 1 to case 4. Modiying the four parameters at the same time to see the temperature profile.

Case 6: Introducing microchannels in the bulk-2.

Results and Discussion

Basecase simulation

For the simulation, an effective heat transfer coefficient of 5W/m^2 • ℃ was applied on top of the package and 500W/m^2 • ℃ on bottom surface of the heatsink. This resulted in the maximum temperature of the stacked IC is around 149℃ .

The simulation temperature profiles of the three architectures are shown in Fig. 5, Fig. 6 and Fig. 7. The temperature contours are from 129℃ to 149℃. From the results of the basecase simulations, it found that the different bonding-architectures has little impact on the maximum temperature of the stacked ICs.

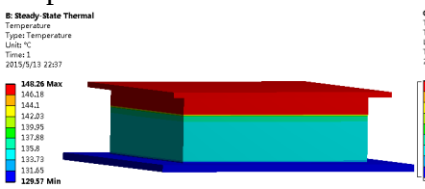


Figure 5 :Temp.Profile of f2f

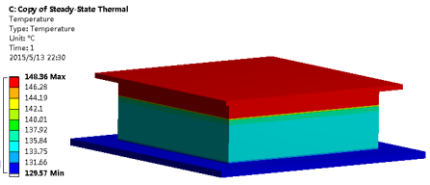


Figure 6 :Temp. Profile of f2b

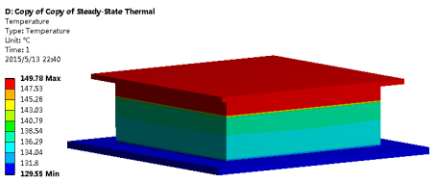


Figure 7 :Temp. Profile of b2b

Other six cases simulation

Case 1: Increasing the thermal conductivity of the bonding-layer to 1W/m • ℃ from 0.2 W/m • ℃ , results in the maximum temperature about 139.33℃ in the face-to-face bonding architecture, 139.43℃ in the back-to-back bonding architecture and 140.86℃ in the face-to-back bonding

architecture. The biggest difference of them is about 1.53℃. It shows that the different bonding architecture has little impact on the maximum temperature.

In the thermal management performance, it has a reduction of around 6% of the maximum temperature in each of the architectures compare to the Basecase.

Case 2: In this case, the maximum temperature of the f2f bonding architecture, the f2b bonding architecture and the b2b bonding architecture are about 146.26℃, 146.36℃ and 147.79℃ respectively. The biggest difference of the three maximum temperature is about 1.53℃, which is the same to the case 1.

From the point of the thermal management performance, it found that there is a little decrease on the maximum temperature on each of the architectures, about 1.3% decrease.

Case 3: In this case, the maximum temperature of the three different bonding architecture is 143.36℃(f2f), 143.46℃(f2b) and 144.56℃(b2b). The difference of the maximum temperature of the three different bonding architecturea is only 1.2℃. It shows the bonding architecture has little impact on the maximum temperature.

From the simulations, it founds that this case has a decrease in the maximum temperature by nearly 4% in all of the three architectures in the thermal management performance.

Case 4: Increasing the thermal conductivity of the package from 36 W/m •℃ to 72W/m •℃ results in the maximum temperature of the three different bonding are 148.26℃(f2f), 148.36℃(f2b) and 149.77℃ (b2b). The biggest difference of them is about 1.51℃. The bonding architecture has little impact on the maximum temperature.

From the point of the thermal management performance, this case has no significant decrease in temperature compared to the case 1. This is because the heat transfer coefficient on the top of the package was ausumed as natural convection.

Case 5: In this case, we study the thermal impact of different bonding architectures on the maximum temperature by combining the case from case 1 to case 4. From the simulations, we find that the maximum temperature of different bonding architecture is 133.72℃ (f2f), 133.82℃ (f2b) and 134.96℃ (b2b) respectively. These three max temperatures are basically equivalent and the biggest temperature difference of them is 1.24℃ .

In the thermal management performance, a case that combining the case from case 1 to case 4 can gets nearly 10% decrease in the maximum temperature in the three different bonding architectures.

Case 6: Microchannel was introduced in the bulk-2 in each of the architectures, as shown in the Fig. 8.

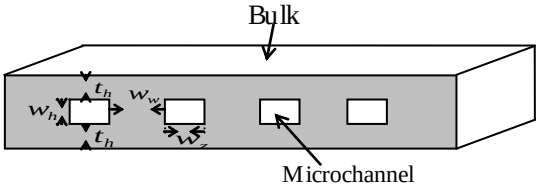


Figure 8:Bulk-2 with microchannels

The microchannels are assumed to be uniformly distributed with identical channel width and height. Liquid coolant flows through the microchannels and carries away the generated heat.

Table 3. Microchannel Cooling Properties

Parameter	Value	Unit
Microchannel Geometry		
Channel height(w_h)	0.3	mm
Channel width(w_z)	0.3	mm
Wall width(w_w)	1.2	mm
Wall height(t_h)	0.35	mm
Microfluidic Cooling Setting		
Coolant Type	Water	
Inlet temperature	25	℃
Pressure inlet	900	Pa
Pressure outlet	0	Pa

The study was conducted with water as a coolant, using an approximate density ρ =1000 kg/m^3 and a constant heat capacity C=4182J/kg·K [12,13,14]. The parameters are shown in Table 3.

From the the results of the simulations, it found that the maximum temperature of different bonding architectures is 54.29℃(f2f), 57.37℃ (f2b) and 132.85℃ (b2b).The maximum temperatures of the face-to-face bonding architecture and face-to-back bonding architecture are are basically equivalent but the maximum temperature of the back-to-back bonding is very different. It shows that the bonding architecture has a major impact on maximum temperature of the stacked IC that with microchannel cooling. The all the simulation results are shown in the Table 4.

Table 4. Max temperature of the different case

	Face-to-face	Face-to-back	Back-to-back
Basecase	148.26℃	148.36℃	149.78℃
Case1	139.33℃	139.43℃	140.86℃
Case2	146.26℃	146.36℃	147.79℃
Case3	143.36℃	143.46℃	144.56℃
Case4	148.26℃	148.36℃	149.77℃
Case5	133.72℃	133.82℃	134.96℃
Case6	54.29℃	57.37℃	132.85℃

From the table 4, it found that the different bonding architecture has little impact on the maximum temperature of the stacked IC when microchannels are not intruduced. But when the microchannels are intruduced, the bonding architecture play a major impact.

From the point of the thermal management performance, it found changing only one single parameter can decrease little the maximum temperature. In the case 5, it can get about 10% decease of the Maximum temperature when changing the five parameters at the same time. When intruducing microchannels, the case 6 can get about 63% decease of the maximum temperature of the face-to-face bonding and the face-to-back bonding, but the back-to-back with about 11.3% decease.

Conclusions

A parametric study and thermal management strategy was conducted on a two die stacked package, which included die1 and die2 on the same substrate. Three different bonding architectures, face-to-face, face-to-back and back-to-back were evaluated. Temperature profiles of the overall package were evaluated with a focus on maximum temperature. Six different cases were assessed from the design and the boundary condition point of view. Of the three bonding architectures evaluated, it found that the different bonding architecture has little impact on the the maximum temperature of the stacked chip that without microchannels. When microchannels are intruduced, the different bonding architecture have a major impact. From the point of the thermal management performance, it found that changing only one single parameter can decrease a little the maximum temperature. The case 6 of intruducing microchannels offered significant improvement in performance. These results can be effectively used as design guidelines in 3D IC thermal management studies.

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