A Design of HD Video Compression and Processing System Based on TMS320DM6467 Processor

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Abstract. This paper proposed a design of HD video compression and processing system due to the process of large amount of data, high flexibility problem during video compression and video processing. This design apply TMS320DM6467 dual-core DaVinci processor. After the research of VPIF interface and video compression, this paper proposed a design which can meet the system requirements.

Introduction

With the development of multimedia technology, the requirements of various fields for the video data acquisition, processing and transmission continues to improve, especially in the field of aerospace [1] [2]. Application of aerospace requirements more stable, flexible, complex system. The TI Company produced several high performance digital signal processors based on DaVinci Technology [3], which were used in many domestic product. Because the DM6467 processor has a wealth of experience in dealing with anti-radiation in the outer space and this processor use ARM core and DSP core architecture [4] which combines the flexible control unit and high performance signal processing unit, this promotes the multi-media development [5]. This paper research the HD video compression and processing system based on TMS320DM6467. This paper designed two different video processing schemes according to the demand of the system.

System Framework

This system process image acquired by CMOS sensor according to the system platform and transfer the data to system platform as shown in Figure 1. This paper proposed the solution to the way of video compression and processing and designed two sets of video processing scheme according to the two different modes of the system requirements.

The video data flow is shown in Figure 2.The CMOS sensor transfer the image data to the signal processing board and encode with YCbCr to YUV and BT.1120 in the signal processing board. Then transfer the video data to the video compression board through the VPIF interface. The video compression board processes the video data according to the instruction, including YUV format conversion, H.264 encoding, image algorithm, transferring the video data to the system platform.

The Design of Video Capturing and Encoding

A. The design of video capture

The system use HD CMOS its output formats meet YCbCr4:2:2. The Y and C component data quantization are both 8bit. The data synchronization clock is 80MHz. this paper have a good design of this non-standard video data real-time transmission system in this section.

The video compression board use one TMS320DM6467 DaVinci processor which has a VPIF interface exclusively for video data transmission as shown in Figure 3. The VPIF interface supports SDTV, HDTV data input/output and RAW capture mode.

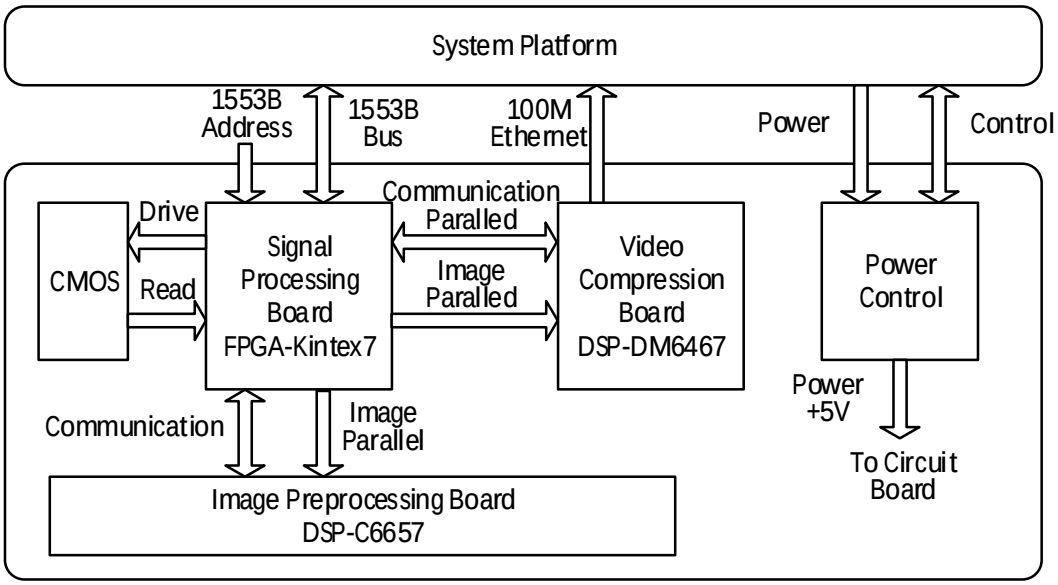

Fig. 1 System Framework

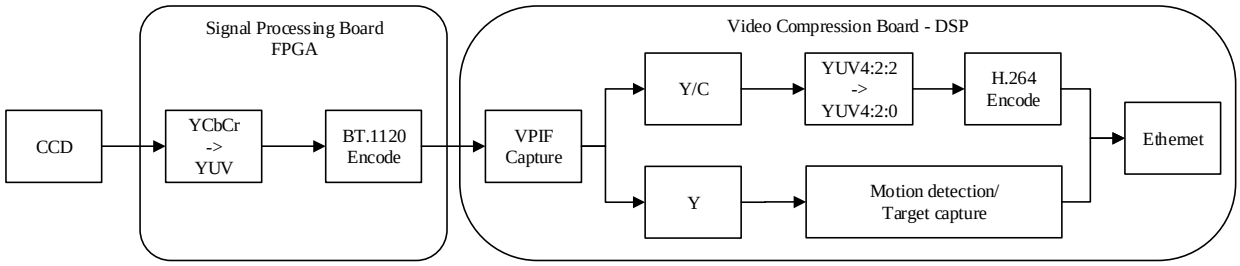

Fig. 2 Data Flow

Because the image resolution of the system is 1920x1080, this system adopts HDTV mode. In this mode the transmission of Y component data and C component data is separated Y component data is transmitted through VPIF channel 0, the C component data is transmitted through VPIF channel 1.

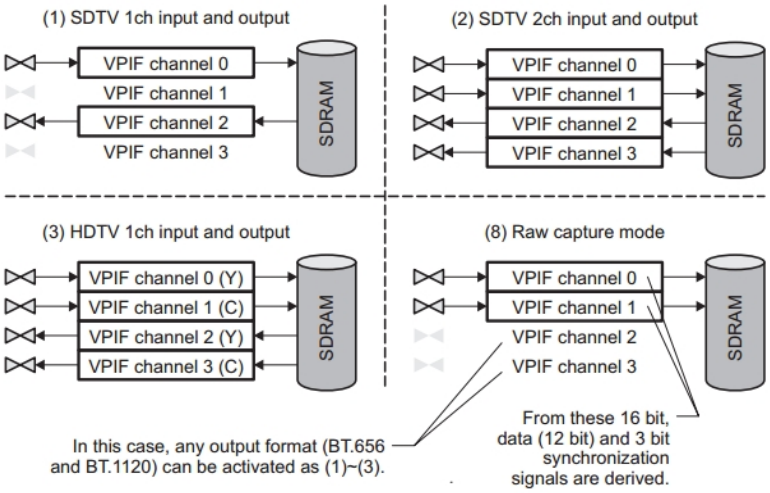

Fig. 3 Input and Output Channels of VPIF

Using the VPIF port has to consider the problem of 27MHz system clock, using ether SDTV input model or HDTV input model as shown in Figure 4. As mentioned in official document, a stable 27MHz system clock was essential due to the real-time transmission of the encoded data. So we use the 27MHz clock source as system clock input.

In the HDTV input mode, the input video format has to be of BT.1120 and the Video Input clock signal uses 74.25MHz or 148.5MHz, but the DSP chip only supports up to 99MHz of the VPIF. So this paper has to adopt 74.25MHz video synchronization clock. In the International Telecommunication Union HDTV related RECOMMENDATION ITU-R BT.1120-8, the standard video progressive scan frame rate supports 60fps, 50 fps, 30fps, 25 fps, 24fps, synchronous clock supports 74.25MHz or 148.25MHz. But the frame rate transmission of this system platform needs to switch among 5fps, 10fps, 20fps, and the synchronous clock needs to be adjusted according to the FPGA part.

In summary, the difficulties of video transmission system lies in the design of synchronous clock rate and video transmission standards does not match, video transmission and standards does not match.

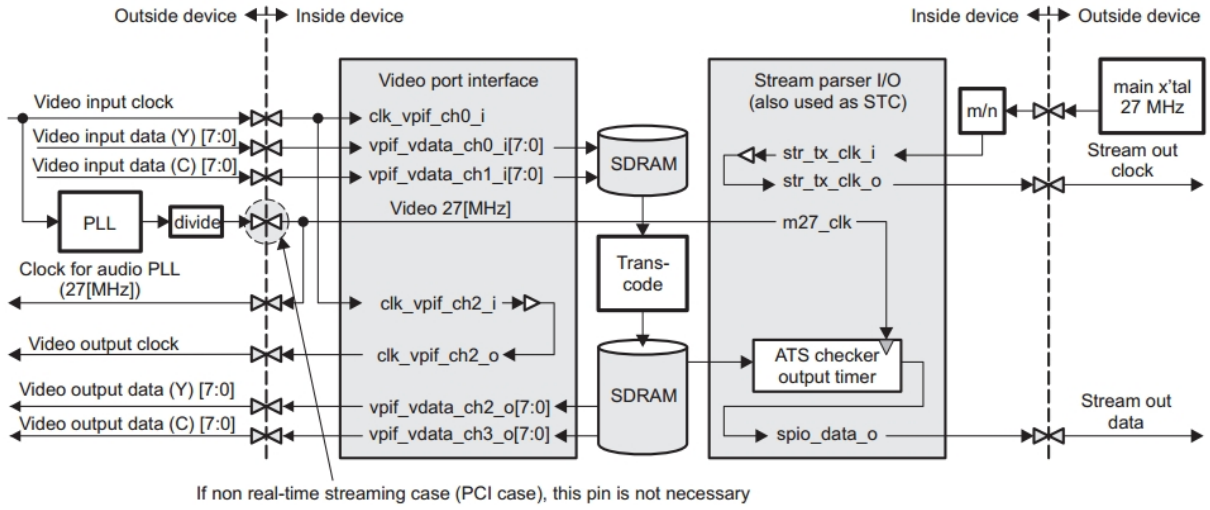

Fig. 4 Clock Control on Video Input and Output with HDTV Encoding

B. BT.1120 Encoding

Because of the synchronous clock of CMOS video data output is 80MHz, the signal processing board has no enough storage space to store the video data locally and send out in the format of BT.1120 format. So the 80MHz video synchronization clock is used to send data. In addition, the format of BT.1120 contain the synchronizing information, the receiver identify the video data by the embedded EAV、SAV synchronous signals. So there is no strictly requirement for video frame. According to the ITU-R BT.1120-8 and TI TMS320DM6467 Digital Media System-on-Chip data, the implement in the FPGA BT.1120 video encoding sequence table is shown in Table 1.

H.264 encoding by two Mealy status machines based on the FPGA. One Mealy status machines used for controlling the switch among the different line of the same image. The other one Mealy status machines used for controlling the switch among the different regions of the same line.

According to BT.1120 data format, the data of the line is divided into five regions, namely, EAV data area, the auxiliary data region, SAV data area, an active data area, and IDLE, using a counter for counting a column value of the image, and according to the counter values to achieve the jump between the states. The timing logic of FPGA is programed according to Table 1.

DSP Video Compression and Processing

Video data in video compression board is processed as shown in Figure 2. One is compressing the Y and C component in H.264 and is output through Ethernet; the other is processing the Y component using image algorithm and the results and Y component is output through Ethernet. The two mode is selected based on the instruction system platform, the same time only has one mode.

When the H.264 compression is essential, VPIF interface receives the Y component and C component. The size of one frame takes 1920X 1080 X 2 bytes. The first 1920 X 1080 bytes are Y

component. The second 1920X 1080 bytes are C component. The format of the video data received by VPIF are YUV4:2:2.Then the data format is converted to YUV4:2:0 and encoded of H.264 using the V4L2 library. Finally the encoded data are send to the system platform through the Ethernet as shown in Figure 5.

Table 1 BT.1120 Timing

Y data stream														
LINE	EAV				Line number data		Error detection		Ancillary data or blanking data	SAV				Digital active line
	3FF	000	000	XYZ	LN0	LN1	YRC0	YRC1		3FF	000	000	XYZ	Y[0]-Y[1919]
1-41	FF	000	000	B6	10	10	10	10	10	FF	000	000	AB	10
42-1121	FF	000	000	9D	10	10	10	10	10	FF	000	000	80	Y
1122-1125	FF	000	000	B6	10	10	10	10	10	FF	000	000	AB	10
C data stream														
LINE	EAV				Line number data		Error detection		Ancillary data or blanking data	SAV				Digital active line
	3FF	000	000	XYZ	LN0	LN1	CRC0	CRC1		3FF	000	000	XYZ	U[0]V[0]-U[959]V[959]
1-41	FF	000	000	B6	80	80	80	80	80	FF	000	000	AB	80
42-1121	FF	000	000	9D	80	80	80	80	80	FF	000	000	80	UV
1122-1125	FF	000	000	B6	80	80	80	80	80	FF	000	000	AB	80
time:	720tclk													1920tclk

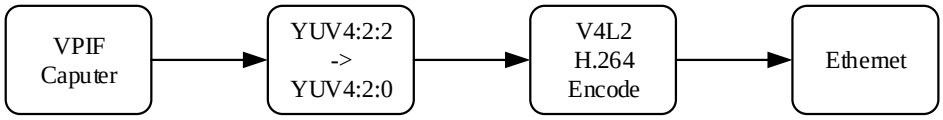

Fig. 5 Framework of H.264 Video Compression

When the Y component is processed using image algorithm, VPIF interface receives the Y component. The size of one frame is 1920X1080 bytes. The moving detection, target capturing algorithm are using on this image and the result are send to the system platform through Ethernet.

System Experiment

The video compression board is shown in Figure 6. This board will send the video data through Ethernet to the system platform, and send the system debugging information through the serial port to the system platform. As shown in Figure 7, the system platform received the debugging information. The Ethernet transmission rate is less than 10Mbps and the video frame rate can also the normal switching. The video decoding software on the system platform is as shown in Figure 8. The software is decoding the HD video which send by the video compression board.

After extensive testing, the system can make the correct data processing in different Telemetry Command and the results can be seen from the video decoding software in system platform.

Summary

This paper design the non-standard video data transmission method based on TMS320DM6467 VPIF interface. A large amount of experiments has proved that this system is stable in it application. According to the system design requirements, two kinds of video data modes are achieved. The whole system has passed the test. The design fully realize all the needs. The parameters are also qualified.

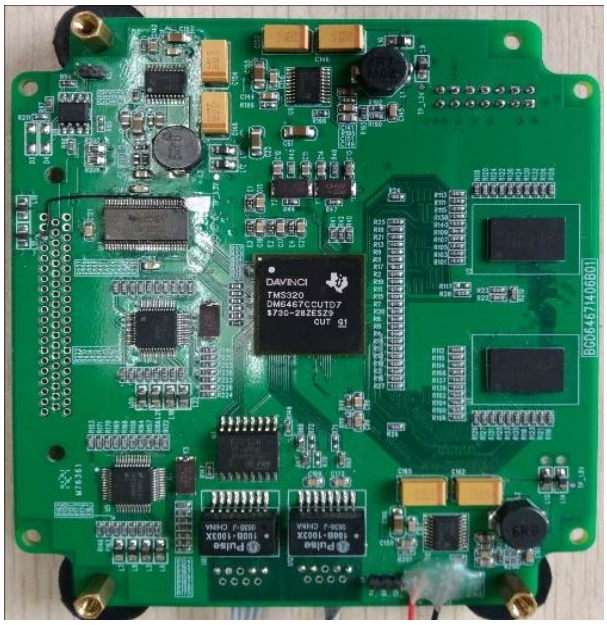

Fig. 6 Video Compression Board

Fig. 7 System Debug Information

Fig. 8 Video Decoding and Playback Software

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