

## The new method of digital circuit fault diagnosis

Yiyang Zhang<sup>1,a</sup>, Yan Dong<sup>2,b</sup>, Dan Liu<sup>3,c</sup>

<sup>1,2,3</sup>changchun engineering technology college, Changchun, 130117, China

<sup>a,b,c</sup>email: 13547021@qq.com

**Keywords:** digital circuit, PSPICE, fault model, fault diagnosis

**Abstract.** The digital circuit is the main part of the current various circuit, any kind of electronic product is inseparable from the digital circuit. Promotes the electronic products greatly improve the performance of digital circuit. Therefore, research on the digital circuit fault diagnosis is of great significance. This article obtains from the digital device failure mode, using PSPICE software has its own function components hard faults and soft fault model is established, and the specific example is given.

### Introduction

With the development of electronic and computer technology, electronic circuit integration degree is increasing day by day, the scale is more and more big, the widely used digital integrated device, some internal and external reasons, often can cause a variety of circuit problem, cause circuit doesn't work.

Any of the components in the circuit malfunction could lead to a part or the entire electronic product failure function failure. In order to maintain a variety of devices and products, to prevent all kinds of accidents, for a variety of electronic products for condition monitoring and fault diagnosis research has very important practical significance in engineering.

### The failure model of the device

Modern digital circuits are made of semiconductor process consisting of several digital integrated device, using the main material is silicon material, also used in high speed circuit compound semiconductor materials such as gallium arsenide, based on the binary digital logic, logic gate is the basic unit. Semiconductor integrated digital device failure mode is mainly has four kinds: short circuit, open circuit, output failure and performance degradation. Refers to the device's output signal output failure errors, concrete can be divided into output for high level all the time, the output is always low level, the output error level; Performance degradation mainly refers to the output delay time increases, driving resistance, etc.

#### Open circuit and short circuit fault model.

On the open pin series resistance values can be used to simulate the open-circuit fault, PSpice software automatically add the interface of the equivalent circuit can realize digital devices and added is used to simulate the open-circuit fault isolation between the big resistance. Fault model is short circuit fault device pins can be directly connected with wire.

#### Output failure model.

Output failure model is divided into: output is always low (high) level and output error level three categories. They all belong to a single fixed failure model (single stuck - at Fault). Single fixed failure model (single stuck - at Fault), also known as a typical (Classical) or Standard (Standard) Fault model. It all failure are described as a single logical gate pin port (or interconnect) short circuit on the Vdd and Vss, fixed on a high logic level is called a fixed 1 fault (Stuck - at - 1), as s - a - 1 (Sa1); On the logic low level is called fixed 0 fault (Stuck - at 0), as s - a - 0 (or Sa0). Single fixed fault is the first used by the research and the fault model, although its effectiveness is not universal, but it is very useful. Single fixed failure model is a restrictive assumptions. In any analysis, assessment, or diagnosis, assuming the same time there is only one failure. The assumption that reduce the complexity of the analysis, make its application is very convenient.

### **Delay fault.**

Delay fault has delay hard and soft failure two kinds of time delay. Which can delay hard fault through Pspice software in the delay element to set the fault circuit (device) of delay time, time delay parameters set by the following statement:

```
X_U9 IN OUT $$G_DGND G_DPWR DELAY PARAMS: DELAY = 50 ns
```

This statement sets the delay time of 50 ns, far beyond the performance parameters of the requirements of all kinds of digital device, thus can realize the time delay of the circuit fault. Delay soft fault can adopt the way of adding components characteristic parameters Settings. In 7404 inverter, for example, in the netlist file add the following components characteristic parameters of the statement:

```
X_U1A OUT $G_DPWR $G_DGND IN 7404 PARAMS: MNTYMXDLY = Y (1, 2, 3, 4)
```

Including MNTYMXDLY is the delay time of the device is installed, its value and time delay characteristics respectively minimum, typical values, maximum and worst case logic simulation.

### **Drive resistance change.**

In PSpice software input file add the following statement set driven resistance value:

```
. OPTIONS DIGDRVF = X
```

```
. OPTIONS DIGDRVZ = Y
```

X, Y, respectively, for the minimum and maximum resistance, the system default value is 20 and 20 k.

Above is of several common faults in the digital devices and model establishment method, but digital device due to the fault type and cause of the failure results, fault number also differ greatly in different systems, thus to establish accurate digital device model, effort. To this end, seeking universal description format of digital devices, makes it easier to build digital device model is more accurate. In PSpice software, digital device description format actually USES a similar to the form of analog devices, its general form is as follows:

```
U < name > < type > ([nin, ngate]) < node * > < time model >
```

```
+ < IO model > [M ntymxdly = < Value >] [IO - level = < Value >]
```

Among them, U < name > is the name of a digital device; < type > ([nin, ngate]) in the type of type name, such as gate, trigger, A/D and D/A converter, pull-up and pulldown resistor, nin said at the input number, ngate said simple door number; < \* > node for the input nodes and output node (there can be multiple); < time model > model name for the device of time; < IO model > name for the device of input/output interface model; [M ntymxdly = < Value >] model for time delay time constant; [IO - level = < Value >] for the choice of interface model level.

## **Use the Model Editor Module Components Soft Fault Model is set up**

Model Editor module is to provide to the user, PSpice software is used to establish a new component Model of the software, the module can support diode (diode), bipolar transistor (bipolar transistor), operational amplifier (the operational amplifier), MOS field effect tube (MOSFET) and so on several kinds of commonly used components. Based on the Model Editor module, on the basis of existing function, put forward using the module modeling method of the components of soft fault. The method on the basis of the existing component Model in PSpice software, combined with the feature of Model Editor module, enabling users to establish all kinds of soft fault Model of components, the use of such a Model method and the use of the PSpice software internal Model base is the same, can be directly call statements using PSpice software, method is very simple, soft fault Model fast and effectively, and failure mode of set is more intuitive, can add it in the fault Model library as the content of the material accumulation, lays the foundation for extending the application range of this method. Soft fault occurs due to components the structure does not change, the establishment of soft fault model can be used when the original components model, just change the parameter values, and each type of component failure mode and the number are fixed, you can use the same components fault model.

Using the Model Editor module components soft fault Model is set up the basic process is shown in figure 1. Can be seen from the flowchart, components of soft fault Model is set up according to

the types of existing component Model library files and the limitation of the function of the Model Editor module itself, you can use several different methods, there are many different between them: for the Model Editor module support type of electronic components, users can refer to the new component Model library file method, according to the component failure mode and the corresponding relation between the parameter value components of the soft fault Model is set up; When you need to Model the components of type Model Editor module does not support when needed a Model library of existing types of components, can copy the component Model defines the statement, in the main program window to copy, according to check the performance of the parameters and the required failure mode set, save the extension set to ".lib", and the output generated \*. Olb files; Can also choose to set up on the basis of the known model library file components of soft fault, this method is simpler, but the file is bigger, because at this time is a kind of components of the model library file contains saved model library files, some of the component model is used. When the system in the simulation, according to \*.net file name defined in the components in the \*. Lib file search and call the needed components model. In practical application, if you want to simulate a certain components all soft fault, the best way is to put on the components of all fault models in the same \*. Lib files, and outputs generated \*. Olb file, so easy to quickly find and call. The caveat is \*. Olb file with the \*. Lib files are need one-to-one, and need to exist in a folder at the same time, both be short of one cannot. In the numerical circuit simulation software Cadence of graphic input module input circuit diagram, the Capture circuit called components model is actually in \*. Olb file search of internal directly. No matter use which kinds of means components of soft fault model is set up, in the \*. Net file name must be defined in the components with identical model defined in the component library file name.

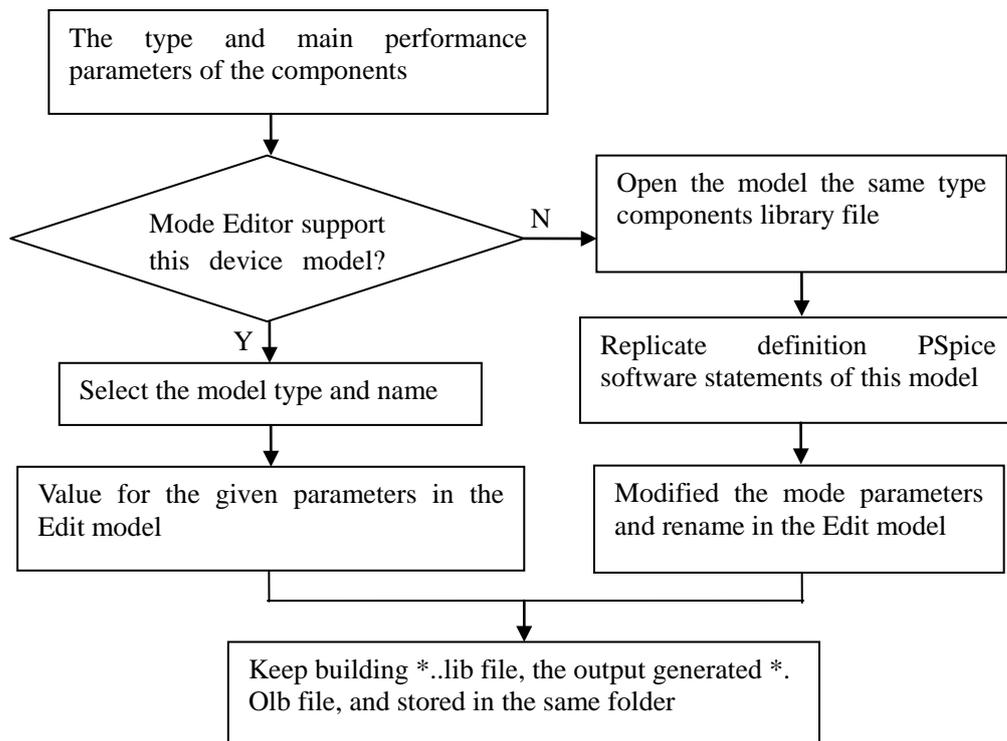


Fig.1 Flow process chart of building component soft-fault model

The following transistors Q2N2222 magnification change, for example to specify soft fault model process:

As a first step, the Model using PSpice software Editor open module library bipolar transistor Q2N2222 belong. Lib, choose Q2N2222 transistor, the Model Text of Model parameters to describe the statement copy;

The second step, the establishment of new \*.lib file, which can be named Q2N2222g.lib.

The third step in Q2N2222g.lib file within the new fault Model is set up, can be named Q2N2222-1, in the Edit Model mode paste Q2N2222 Model statements, changed the parameters of  $\beta = 255.9 = 25.59$ , other failure Model establishment method same as above;

The fourth step, save Q2N2222g.lib file, and the output generated Q2N2222g.olb files, both in the same folder.

So you get the transistor Q2N2222 magnification change all of the soft fault model.

## **New Approach of Fault Knowledge Acquisition**

At present more mature intelligent fault diagnosis technique of expert system and fault dictionary method. Use of fault diagnosis expert system of the basic process is: through the computer acquisition was diagnosed object information, and then the integrated use of various rules (expert experience) to a series of reasoning, calls to various applications at any time when necessary, the process of running by the user to obtain the necessary information, to quickly find the final failure or the most likely failure, by the user to confirm again. Fault dictionary method in the diagnosis of the basic idea is: first of all, extract the circuit (system) in the circuit characteristics of all kinds of fault condition, and then will be the corresponding relation and fault characteristics listed in a dictionary. In the real diagnosis, as long as the real time characteristics of extraction circuit (system), you can find out the corresponding fault from fault dictionary.

From the implementation process of expert system and fault dictionary method can be seen that they have certain limitations in terms of knowledge acquisition, it is a must rely on the heuristic knowledge of experts in the field to build knowledge base; Second, each expert system and fault dictionary can only work for a specific circuit systems.

In this article, through the in-depth study of fault knowledge acquisition methods, put forward the strategies of the circuitry underlying obtain fault knowledge, achieve the innovation of the fault knowledge acquisition method, effectively overcome the above two shortcomings.

From the most basic unit - circuit components, obtain the deep knowledge of electronic circuit, away from the dependence on expert experience knowledge. The experience of the experts can improve the efficiency of fault diagnosis, but it is not necessarily effective. Using PSpice software simulation to obtain fault knowledge, this paper is based on the deep knowledge of the whole circuit of circuit simulation analysis, the process of acquiring fault knowledge. Specific steps are as follows: first of all, according to the various components of fault model specific method, all components of practical fault model are established within the PSpice software; Secondly, combining with PSpice software netlist file input circuit description statement, and the characteristics of the model describes the statement, through process control components fault description statement on normal components described replacement, generate new fault netlist file; Finally, recycling program control command line to start the PSpice software simulation program, A/D to the failure of the electrical network file load simulation, simulation results to extract data, to realize automatic fault knowledge acquisition.

## **Conclusion**

This article provides a method of component failure model is established in the new object with the diagnosis of different fault model library, constantly enrich the features of good generality, scalability and portability, and can be applied to different types of digital circuit, enlarge its application scope, prolong service life, efficient fee than.

## **References**

[1] Katya Asparuhova, Tsvetana Grigorova. IGBT Behavioral PSPICE Model. PROC.25th Instrumentation Conference on Microelectronics (MIEL2006), Belgrade, Serbia and Montenegro, MAY, 2006:14-17.

- [2] S Reynolds. Vacuum-Tube Models for PSpice Simulations[J]. Glass Audio, 1993, 5(4): 17-23.
- [3] Mehran Aminian, Farzan Aminian. Neural-Network Based Analog-Circuit Fault Diagnosis Using Wavelet Transform as Preprocessor, IEEE Trans. on CAS-II: Analog and Digital Signal Processing, 2000, 47(2): 151-156.
- [4] Jinyan Cai, Alam. M.S. An algorithm for dividing ambiguity sets for analog fault dictionary. MWSCAS-2002, 2002(1): 89-92.