

# The Design Of High-precision, High-capacity, Multi-channel Synchronous Data Acquisition System Based On STM32

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**Abstract.** In recent years, with the development of computer and electronic technology, it provides the necessary conditions for the collection of data and the development and application of storage systems. Therefore, combining with the current actual demands, this study analysis and designs the high-precision, high-capacity, multi-channel synchronous data acquisition and storage system based on STM32 including the specific functional requirements of the system hardware and software selection, in order to provide more opportunities for further development of the data acquisition and storage system.

## Introduction

During the design process of the system, the most critical is to achieve three functions including data acquisition, storage and transmission. The accuracy and speed of acquisition should be considered in the design of data acquisition, the former is mainly reflected by the significant digits through the A/D conversion chip, and the latter is mainly reflected by means of sampling rate. Currently, the highest sampling rate of A/D has reached 1.5 Gb. The sampling median (resolution), sampling rate and sampling channels are mainly considered when selecting A/D converter chip. Following demands are required for A/D acquisition: There are three or more channels with synchronous acquisition, the sampling rate of each channel is between 0-100KSPS and the precision reaches to 12 bit at least. The design chosen AD7656 based on these demands and its performance indicators are as follows: (1). Input channels: support 6-channel synchronous acquisition; (2) Sampling rate: up to 250KSPS; (3) The sample median: 16 Bit.

In the design of data storage, the most critical is storage capacity and speed. The cost must be considered when selecting large-capacity memory because it will increase a lot with storage capacity increasing. In this design, the requirement of storage capacity is relatively low. It only needs to reach to more than 100M. In the presence of the storage speed, not only the efficiency of chip erase and writing should be considered but also the program algorithm has a close relationship with the storage speed, which includes the designs of broken block processing algorithm, the file system and the sector R/W management algorithm. In the condition of high-speed, real-time, continuous acquisition and storage, on the one hand, it requires the system to uninterrupted signal acquisition; on the other hand, it requires achieving real-time data storage, otherwise it will cause data loss. Therefore, in this design, using the double buffer alternating storage mode under 100KSPS sampling rate and over 840 bytes buffer in order to ensure the collected data can be finished In the high-speed, real-time, continuous acquisition and storage of intelligence Under conditions, on the one hand it requires the system to uninterrupted signal Acquisition, on the other hand required to achieve real-time data store Storage, otherwise it will cause data loss. Therefore, in the present design, using the double buffer alternating storage mode, under 100KSPS sampling rate, the size of the buffer should be super Over 840 bytes, in order to ensure that the data collected can be saved to flash completely.

In the design of data transmission, the system is generally used in the offline, accomplishes real-time field data collection and storage quickly and it recovers memory in the end. The memory will be measured by computer processing and reproduce information. Although without the need for real-time transmission of data, a large amount of data makes RS232/485 can not meet the actual

needs of speed in the subsequent data reading and processing. Therefore, USB becomes the preferred choice with the advanced features of its plug and play, hot-swappable and high transmission rate in the data transmission design.

### **The hardware design of system**

**The Microprocessor.** The central part of this system hardware design is MCU and USB controllers, we can achieve communication fast between upper and lower machine in the both combination so that the PC will gain data that system has collected. Currently, the MCU has exceeded more than a thousand species, they are divided into three categories including 8-bit, 16-bit and 32-bit according to width of data bus. Combining with its actual needs, the design of this system chose STM32 series processor based on ARM Cortex-M3. STM32 series processor has excellent performance, ultra-low power, high integration with a reset circuit and accurate RC oscillator and provides a rich of peripherals and USB interfaces in order to develop USB conveniently. What's more, it provides simple-to-use tools for free.

**A/D Conversion Chip.** Although STM32F103ZE supports 21-channel acquisition with three synchronous ADCs it can not meet the system design claims as a result of only achieving 3-channel synchronous acquisition. Therefore, the design selected AD7656 produced by ADI company, which is a SAR type A/D chip with 16-bit. AD7656 contains 6 internal A/D converters that maximum conversion rate is up to 250 KSPS and converts by 3 $\mu$ s. It supports 6-channel synchronous acquisition. The built-in low noise, wideband sample holding amplifier (T/H) can be used to handle input signal up to 4.5MHz and connect with MCU, DSP or connect a plurality of ADC to single serial interface.

**The Peripheral Memory.** Flash memories are divided into two categories including NAND and NOR according to their underlying technology structure with the characteristics of large capacity, low power consumption and easy to clear. There is very high demand for the data acquisition and storage system in storage speed. Considering the system capacity, cost, hardware device, this design selected Nand Flash K9F1G08UOB, which consisted of 1024 blocks, 64 pages, a total of 132 bytes. The total storage capacity is 1GB+32M and there are 64 bytes of redundant bytes on every page of memory.

**The control circuit of USB.** The MCU of STM32 can be connected by its slave USB controller which conforms to USB2.0 full-speed device technique standard. The slave USB controller provides hardware interface for STM32F103 and USB to exchange data. The data transfer between PC and STM32 by sharing a dedicated data buffer. At the same time, the data buffer can be accessed directly by USB peripherals. When the USB module is in non-working state, it can set USB into low-power mode by writing to control register and it doesn't consume any static current. When you need USB to work, you can wake up USB in low-power mode by detecting the data transfer in USB.

### **The software design of system**

The system needs to complete three basic functions including data acquisition, data storage and data transfer. The three parts achieve coordinated operation under the monitoring and task scheduling of system. Firstly, in the data acquisition part, turn the timer when detecting external trigger signal. The timer interrupt processing unit mainly complete 6-channel simultaneous acquisition of a point each workflow. Close the timer when acquisition time is reached, namely stop A/D conversion. Secondly, in real-time storage part, it needs to storage data for real-time due to uninterrupted signal acquisition; otherwise it will make data lost so that results in data incompletely. The storage procedure adopts double buffer mode. Finally, in the USB communication section, USB controller achieves data exchange between the port and dedicated buffer by an internal 16-bit register. When detecting USB interrupt request, send or receive appropriate handshake packet data according to the direction of transmission for needs after data transmission is completed. At the end, USB controller will trigger interruption associated with endpoint by reading the status register.

The process of software design is following: At the first, system begins to initialize when it is power-on, then set appropriate acquisition time through the upper machine. The acquisition time should be shorter when the acquisition is comparative high. If the flash is empty, start A/D conversion by an external trigger signal, if not, user can read the file in flash by the USB port from upper machine. User also can clear the flash by external button. Stop A/D conversion when it reaches the acquisition time in advance, user can read the data file by USB port in the way of connecting the system and PC by USB cable. However, in the process of data acquisition and storage, the USB is not allowed to be accessed.

## **Summary**

This paper studied the high-precision, high-capacity and multi-channel synchronous data acquisition system based on STM32. At the same time, it introduced the main function requirements, the choice and characteristics of corresponding chips, acquisition, storage, communications transport and necessary peripheral circuits in the hardware design so that it will provide some experience for the further development of data acquisition and storage system.

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