A Design of M-LVDS Transmitter IP

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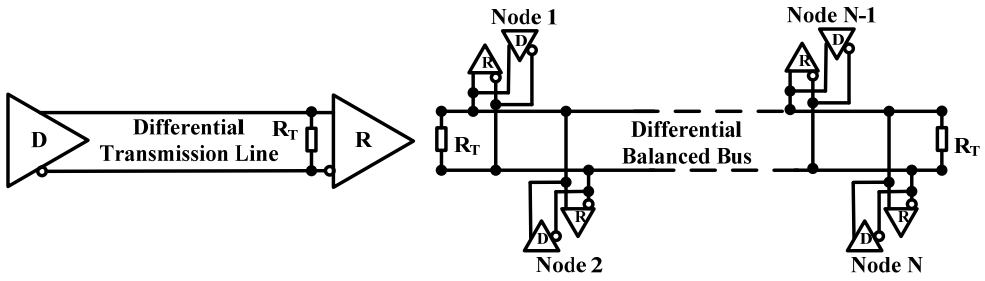
Keywords: M_LVDS; Transmitter IP; Wide-Swing Current Mirror; Interface.

Abstract. Multipoint low voltage differential signaling (M-LVDS) [1], who's electrical parameters meet the requirements of ANSI/TIA/EIA-899 standard, is a widely used technology in multipoint interconnection. Through the study of the standard, the wide-swing current mirror technology was proposed to satisfy the requirements of large current by the M-LVDS transmitter in circuit design; the analog power supply ring and the digital power supply ring were separated in layout design, and more contacts were added reasonably between ground and substrate, thus, a better noise performance was obtained; a bias module can drive four driver module accordingly through separating the voltage/current bias circuit and the driver circuit in two parts in layout level, which will increase the reuse of the transmitter IP.

Introduction

Various interface standards were proposed to solve the different transmission rate in/out the chip and reduce power consumption at the same time. Low voltage differential signaling (LVDS) [2] technology is such a standard with high speed, low power consumption and low cost. It is widely used in point to point transmission structure (See Fig.1.a). However multipoint interconnection (See Fig.1.b) is another common transmission structure that LVDS technology is inapplicability, thus the M-LVDS technology bases on the LVDS technology was proposed in 2001 to solve such application situation.



(a) Point-to-point structure (b) Multipoint interconnection structure

Fig.1 Transmission network topology

There are two difficult points in M-LVDS transmitter IP design, large driver current and low noise margin. The wide-swing current mirror technology was proposed to satisfy the requirements of large current by the M-LVDS transmitter IP in circuit design; the analog power supply ring and the digital power supply ring were separated in layout design, and more contactors were added reasonably between ground and substrate, thus, a better noise performance was obtained. What's more, a bias module can drive four driver modules accordingly through separating the voltage/current bias circuit and the driver circuit in two parts in layout level, which will increase reusability of the transmitter IP.

This paper first presents advantages and disadvantages of M-LVDS transmitter. The Wide-swing current mirror technology is then discussed. The design of Transmitter IP and summary follow.

Advantages and Disadvantages of M-LVDS Transmitter

According to TIA/EIA-899 standard, the M-LVDS transmitter generates a signal with 480mV to 650 mV difference amplitude and the common-mode voltage range is 0.3V to 2.1V. The slew time of

the transmission signal must be greater than 1ns (The time costs that the difference amplitude raise/fall from 10% to 90%, including rise and fall time) and up to half of the unit interval (t_{UI}). Based on skew time (≥1ns), the maximum signal rate is 500Mbps in the standard.

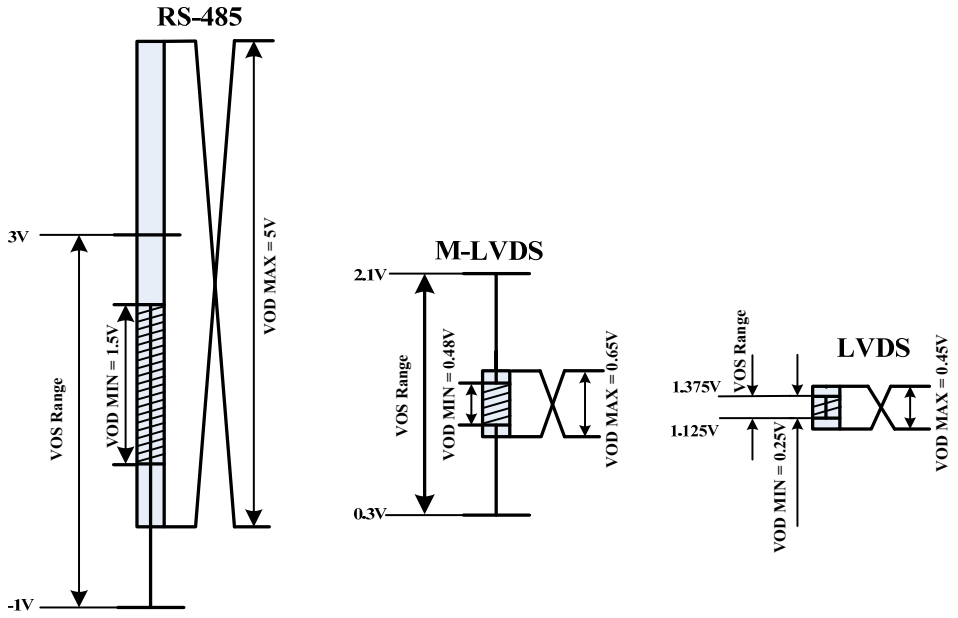


Fig.2 Comparison of Vod and Vos in different drivers of three protocols

It is performance as a heavier load if the transmitter has been connected with double-ended termination network, so there must be a stronger drive to keep the signal amplitude needed. Compared with LVDS transmitter, the M-LVDS transmitter has a greater driving capacity (See Fig.2), thus it is capable of driving double-terminated multi-point network signal. In addition, for other topologies except point to point structure, the LVDS transmitter is also difficult to use for the conversion time from 100ps to several hundred ps, the M-LVDS transmitter is still appropriate.

Compared with the RS-485[3] transmitter, the M-LVDS transmitter provides smaller signal amplitude (See Fig.2), so as to reduce the power consumption and electromagnetic interference (EMI). And lower signal amplitude allows higher signal transmission rate (or signal frequency). The M-LVDS transmitter has higher signal rate (≤500Mbps) than the RS-485 transmitter(Few chip can reach the rate of 30Mbps to 50Mbps). However, M-LVDS has the advantages of high speed, low power consumption, and low EMI are at the costs of reduce the noise tolerance [4, 5].

Wide-Swing Current Mirror Technology

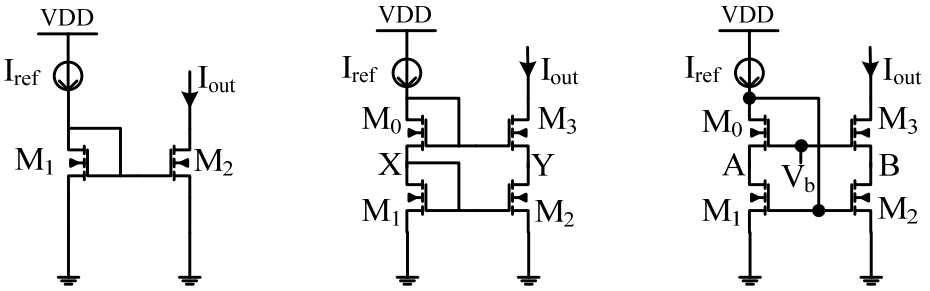
For the basic current mirror (See Fig.3.a), when the modulation effect of the channel length is not considered, the Iout can be copied by I1, but the effect cannot be ignored in practical application, thus:

$$\frac{I_{D1}}{I_{D2}} = \frac{(W/L)_2}{(W/L)_1} \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \tag{1}$$

Therefore, the replication of the current has great error. Especially in the deep sub micron and nano technology, in order to get the smallest device capacitance, the minimum channel length is used. The smaller the L, the I_{DS} is affected by the short channel effect seriously, and the greater the error.

In order to solve the effect of channel length modulation, the cascode current mirror (See Fig.3.b) has been widely used because of the isolation of the common gate transistor. As shown in the Fig.3.b, the M3 plays as a isolated common gate transistor, which makes the leakage voltage of the M2 very small, thus the I_{out} can be copied from the I_1 accurately, as long as the V_{DS} and physical size are same of M_1 and M_2. However, the current mirror is used to consume more voltage to obtain high accuracy。The minimum output voltage is：

$$V_{out} = V_{on3} + V_{on2} + V_{TH2} \tag{2}$$



(a) Basic current mirror (b) Cascade current mirror (c) low voltage cascode current mirror

Fig.3 Current mirror

In order to eliminate the contradiction between the accuracy and the redundancy, the low voltage cascode current mirror structure with the input and output short (Also called wide-swing current mirror[6], See Fig.3.c) is used. When all the MOS transistors work in the saturation region, the cascode transistor M_3 and M_2, consumption minimum redundancy, and the minimum output voltage is:

$$V_{out}=V_{on3}+V_{on2} \tag{3}$$

And the isolation of the cascade structure, the V_b is less affected by the outside world and the V_b is:

$$V_b=\frac{\Delta V_{out}}{(g_{m2}+g_{mb2})\ r_{o2}} \tag{4}$$

Design of Transmitter IP

The function of M-LVDS transmitter is to convert the input CMOS level or TTL level signal into a low swing, low noise and high conversion rate LVDS signal. The whole transmitter IP is composed of a voltage converter, a single-to-differential converter with data buffer, a voltage/current bias module and an output drive module (See in Fig.4).

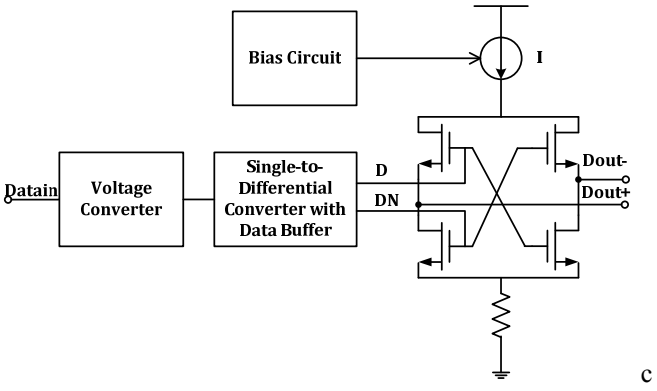


Fig.4 Structure of the transmitter IP

Circuit design. The voltage converter (See Fig.5.) is to convert the 1.2V core voltage to the 3.3V port voltage by the cross coupled NMOS transistor, and then hand over the single to the single-to-differential converter with data buffer (See Fig.6.).

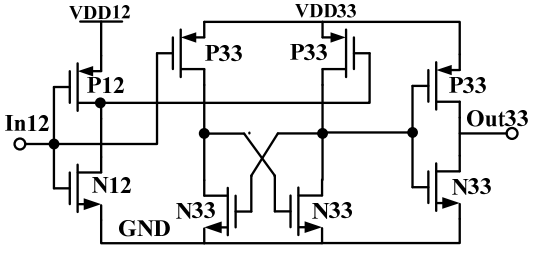


Fig.5 Voltage converter

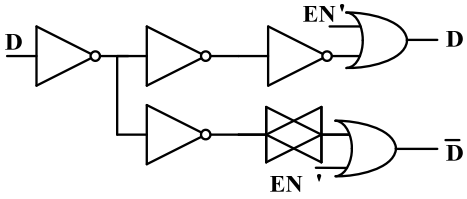


Fig.6 Single-to-differential converter with data buffer

The main function of single-to-differential converter with data buffer is to convert single signal into differential signal, and enhance driving ability. The function of the transmission gate is to make the two signals of difference with appropriate delay time.

The voltage/current bias module (See Fig.7) consists with a band-gap reference, a voltage-current converter and a wide-swing current mirror. According to simulation, the band-gap reference generates a 1.24V reference voltage. In the whole temperature range from -55 ℃ to 125 ℃ ,it only changes 4mV, which meet the requirements of M-LVDS transmitter IP. The most accurate way to convert voltage to current is to use the op amp. In order to ensure stable of output voltage swing, the swing of R must be controlled within 15%. Wide swing current mirror ensures the reference current is amplified to the desired range accurately.

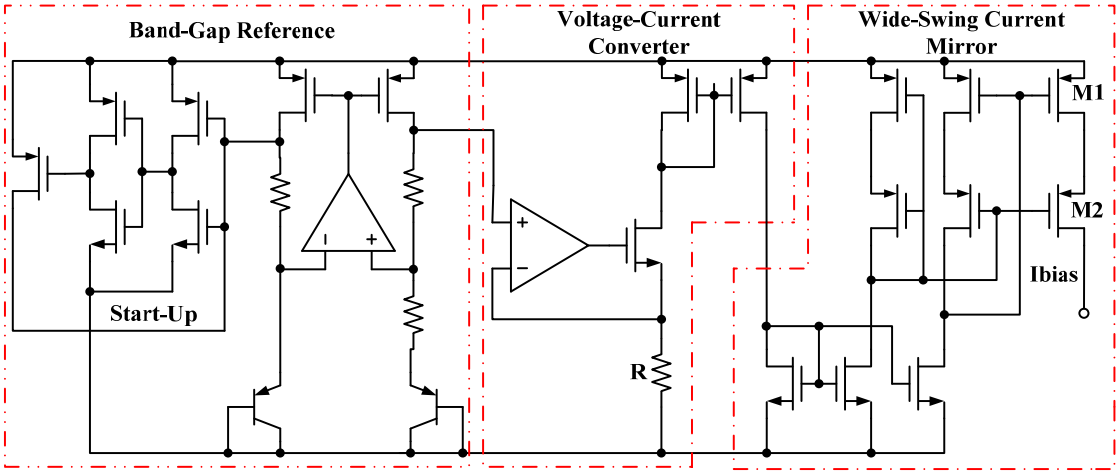


Fig.7 Voltage/current bias module

Layout design. The layout of the IP is shown in Fig.8. In the layout design, the following factors were considered:

1. The placement of the modules are coincident with the direction of the signal;
2. The P diffusion isolation region were added between different modules to improve the latch up immunity of the IP;
3. Guarantee the symmetry of the IP;
4. The reference circuit is far from the digital circuit and the large size output transistors are placed in the periphery;
5. The analog power supply ring and the digital power supply ring were separated, and more contacts were added reasonably between ground and substrate, thereby a better noise performance was obtained.

The IP occupies a die area of 330μm x 211μm

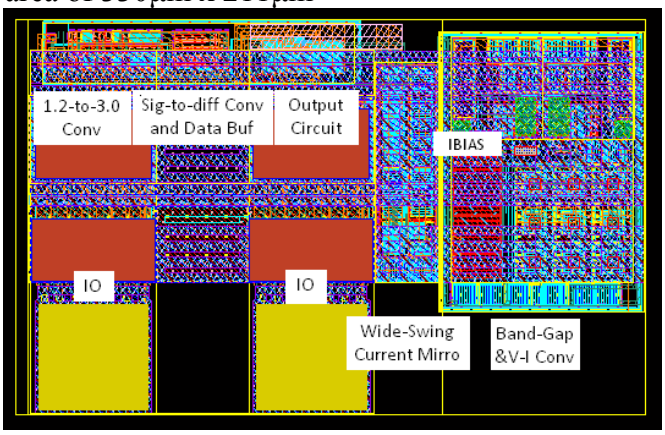


Fig.8 Layout of the M-LVDS transmitter IP

Simulation. The IP was designed in SMIC 130nm CMOS standard technology and simulated with Cadence spectre. The input signal rate is 500Mbps. There were three kinds of extreme conditions "slowest", "typical" and "fastest" had been simulated, the specific configuration is as follows:

1) The slowest: the corner was SS, the temperature was 125℃, the power supply voltage was 3V;
2) The typical: the corner was TT, the temperature was 27℃, the power supply voltage was 3.3V;
3) The fastest: the corner was FF, the temperature was -55℃, the power supply voltage was 3.6V;

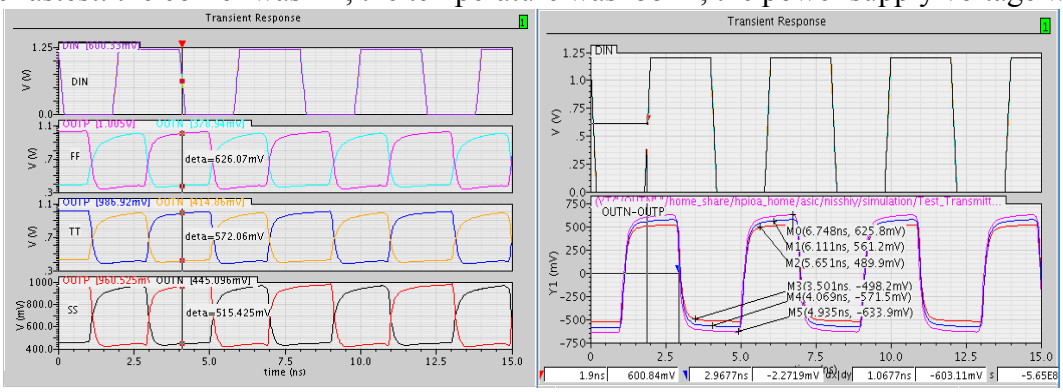


Fig.9 Simulation results

Simulation results can be seen in the Fig.9 When the input data rate is 500Mb/s , the signal can be transferred effective. The output signal swing is about 572.06mV (typical), the common mode voltage is about 750mV, meeting the requirements of the TIA/EIA-899 standard. The total power consumption of the IP is about 80mW.

Summary

M-LVDS is a LVDS technology for multi point data transmission, which has low swing and current mode output driver. And it has very low noise and low power consumption in a wide range. An integrated M-LVDS transmitter IP was designed and fabricated in SMIC 130nm CMOS standard technology. The IP can operate at a high speed of 400Mbps and supports point-to-multipoint structure and there are 32 receivers can be driven at most at one time. The IP can be used in point-to-point data transmission at physical layer of communication system or data transmission on SoC.

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