Simulation of 1.0 μm CMOS Baseline Process at AEMD of Shanghai Jiao Tong University

Didi Ma[1, a], Xiaodong Wang[2, b], Yun Shen[2,c] and Xiulan Cheng[3, d*]

[1,2]School of microelectronics, Shanghai Jiao Tong University, Shanghai 201100, China;

[3]AEMD, Shanghai Jiao Tong University, Shanghai 201100, China.

[a]didiqlx@sjtu.edu.cn, [b]mrhbcf@sjtu.edu.cn, [c]shenyun68@sjtu.edu.cn,
*[d]xlcheng@sjtu.edu.cn(Corresponding author)

Keywords: CMOS baseline process, semiconductor device, TCAD simulation, electrical test structure, six-inch baseline run.

Abstract. A standard 1.0μm CMOS process are developed at AEMD (Center for Advanced Electronic Materials and Devices), which is a public platform about advanced micro-nano fabrication. The process supports 1.0 μm twin well technology, with double poly-Si, double metal, and defines the standard process modules in the micro lab. Process and simulation data details are presented with the electrical test structure and device characterization for the first six-inch baseline run.

Introduction

In recent years, the smallest feature size of typical CMOS integrated circuit reduced rapidly, leading to more and more intensive complex circuit [1]. The complexity of the product circuit is almost useless to monitor or debug manufacturing process. Therefore, the test structure is often made with these products, which will be in a much more timely way to measure circuit or fabrication process of specific information. A CMOS baseline definition for a Micro-Nano fabricaiton lab is very necessary to evaluate the process capability and stabilibity, monitor the process contaminations. The most successful example is Nanolab at University of California (UC) at Berkeley [2]. This lab has been supported VLSI silicon MOS technology, and it's facilities has be opening since 1983. The first CMOS baseline report in UC lab was about 2 μm Nwell, double gate and metal process;then a 1.3 μm process was developed [3]. This process further was refined on 4 inches substrate in 2000 [4], and then was realized on 6 inches substrate [5]. Next, the 0.35μm CMOS process was developed [6]. In addition, by adjusting the dose and equipment parameters, it implemented the three layers of metal process, satisfying the demands of IC chip test [7].

In this project, the 1.0μm CMOS test structures are placed in scribe line and produced with target circuit. This project was developed in an opening Micro-Nano fabricaiton lab, named AEMD (Center for Advanced Electronic Materials and Devices) at Shanghai Jiao Tong University. The center with a lot of micro-nano fabriction facilities intends to build university-level micro-nano fabrication and testing platform and perform the state of art research on semiconductor materials and devices, optoelectronic materials and devices, MEMS technologies, bio-nanotechnology, and IC chip packaging technologies. The micro-nano fabrication process in the center could be customerized with a wide range of needs and recipes. The process which supports 1 μm twin well technology, with double poly-Si, double metal, was designed to define standard process modules in the lab. , and provides the technology reference for different projects to determine the starting point of the research, and to allow the designer to feedback the circuit performance results to the process, improving the process. In addition, it can monitor the process contaminations for various process equipments. Through the test data, the process problem could be found and modified quickly. The NMOS and PMOS with 1 μm gate length are simulated with TCAD software, and the fabrication process is designed in this paper.

Process Design

Test structure

CMOS baseline development is primarily to test the structure of the formulation, manufacturing, testing and simulation. Test structures are used for device, circuit and process parameter extraction, as well as random fault and reliability testing. These categories have been designed by David Rodriguez [8].

Process design

This project aims to design a double well, double gate and two layers of metal standard 1.0 μm CMOS process. The process has 8 implantation steps and 14 lithography steps; however, the number of the masks applied is 12. Except ion implantation process, all the process steps will be completed in AEMD lab. The starting material is 24-36 Ω-cm p-type, <100> wafer. The 1 μm (the smallest) N- and P- channel MOSFETs can be fabricated with punch-through implants. The process also contains N-field and P-field implants. Many main typical parameters are simulated, such as V_T, Xj, R, T_{OX}, γ.

Process Flow and Cross Sections

Process flow includes lithography, oxidation, ion implantation process and so on. The process of manufacturing level is mainly determined by the ability of lithography, so lithography is very important. A critical processes flow with device cross sections are shown in Fig. 1 a-d. All process steps are accomplished in the AEMD except ion implantation.

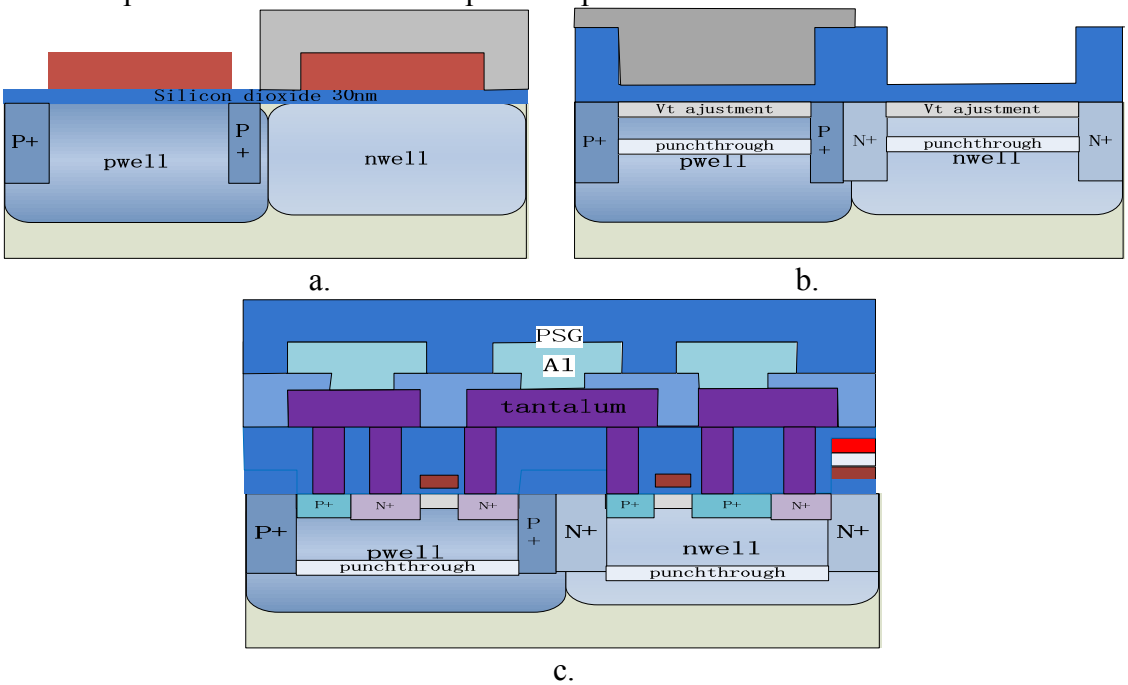

Fig. 1 Process flow steps

a. N-well, P-well and active area formation b. LOCOS and channel Iiplants c. Gate Formationd and Metallization

CMOS baseline structures are general placed in the scribe lane. This will not affect the normal circuit in the die, and shall not affect the test. Moreover, researchers can utilize the drop-in area for their own devices. The topic use the most basic circuit in this time, so test structures are also arranged in the die area, as shown in Fig. 2. In this fig, the test structures are marked out with red doted line.

Simulation Result

Devices simulation use Silvaco TCAD software. Device model in the simulation are two-dimensional, and the width of the default is 1 μm.

The simulated (ATHENA) and measured doping profiles under the gate oxide for both types of transistors (L=1μm) are simulated. Taking the NMOS for example, show the simulation results. Fig. 3 shows the device structure. It can be seen the material we used and a red line which is the PN

junction. The diagram in Fig. 4 represents the concentration of ion implantation. The turning point is the depth of ion implantation, named junction depth Xj, in S/D area. By the 'extract' commend, the Xj value concluded is 0.274214 μm. Device was simulated by ATLAS to output the function character, as shown Fig. 5 and Fig. 6. In Fig. 6, gate voltage are respectively 1V, 2V, 3V from bottom to top.

For making standard cell, it needs multiply threshold voltage value (V_T). We know that the calculation formula is shown as the below [9]

$$V_T=V_{T0}+\gamma\left(\sqrt{|(-2)\phi_F+V_{SB}|}-\sqrt{|2\phi_F|}\right). \quad (1)$$

Therefore, we can vary the value of V_{SB} to change V_T. As a result, we simulate the device to get the drain current vs. gate voltage curve at varying substrate bias (-1V,-2V,-3V from left to right), as shown in Fig. 7. By extracting the data, threshold voltage can be calculated. The threshold voltage value is respectively nvt1=0.516872V，nvt2=0.825124V，nvt3=1.05205V.

It is important to pay attention to the contact of metal and semiconductor, which can affect the voltage. Since different materials own different work function, the metal and semiconductor contact will form two forms [10]. One is the rectifying contact, named schottky diode, working like pn junction diode, forming barrier layer; the other one is the Ohmic contact, like a low resistance, not affecting the current voltage characteristic, forming non barrier layer. In practice, the latter case is what we want. Fig. 8 shows the contact in NMOS. It can be known that if the contact between NMOS and metal is one type contact, the contact between PMOS and metal is another type contact. Therefore, the problem is solved by painting the bottom with Ti, before the aluminum deposition.

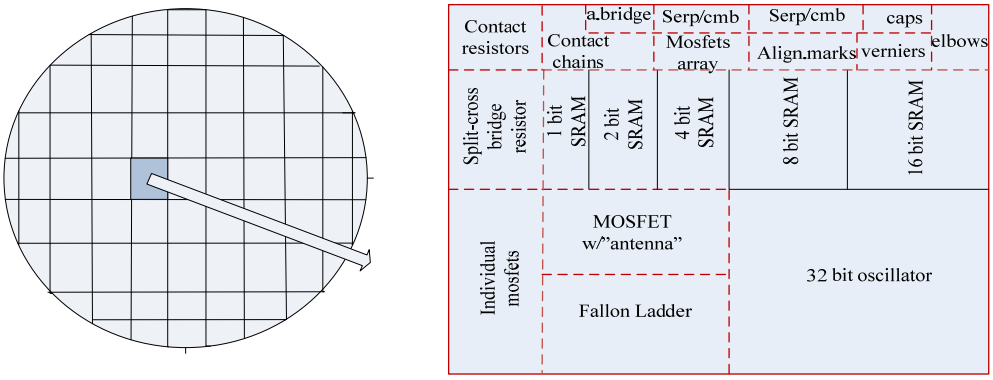

Fig. 2 Arrangement of test structures

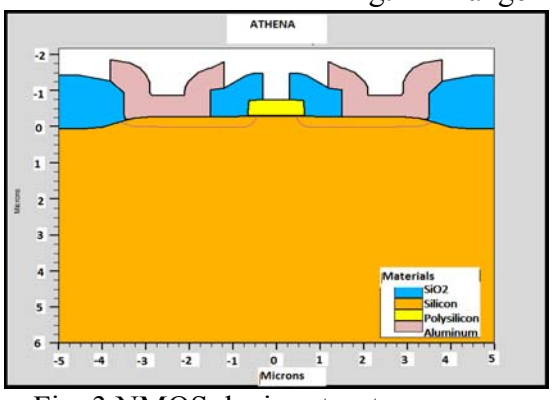

Fig. 3 NMOS device structure

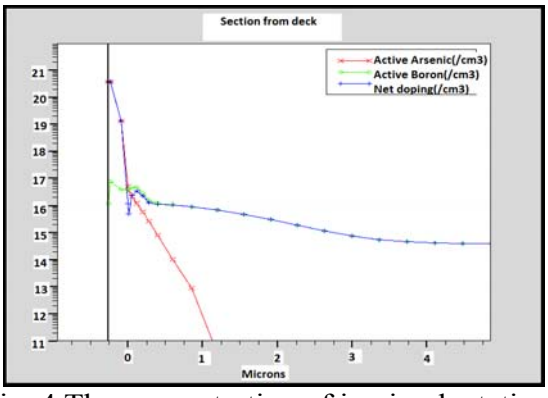

Fig. 4 The concentration of ion implantation

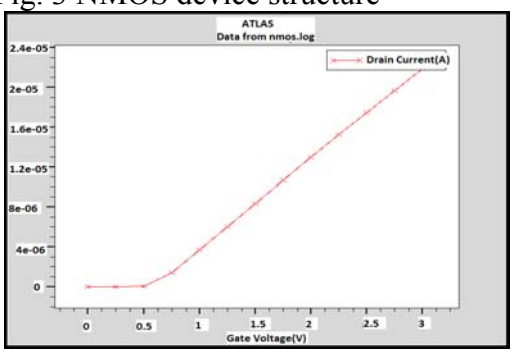

Fig. 5 NMOS (W/L=1/1) I_d-V_g curve.

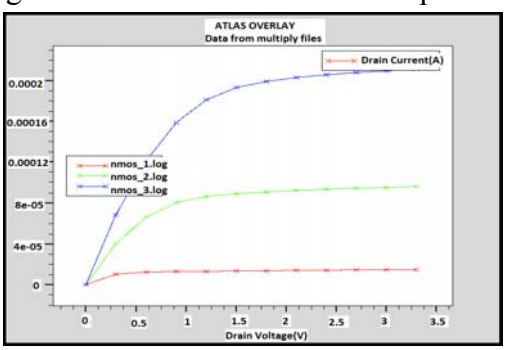

Fig. 6 NMOS (W/L=1/1) I_d-V_d curves.

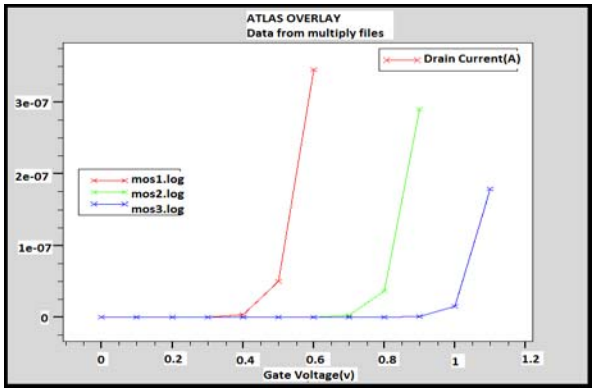

Fig. 7 NMOS (W/L=10/1) Id-Vd curves with differen substrate bias

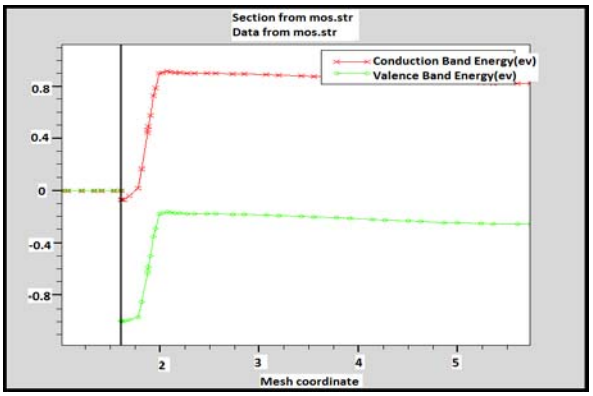

Fig. 8 Metal and semiconductor band diagram

Summary

A 1μm CMOS baseline process was developing at AEMD of SJTU. Device structures were designed and the electrical performance were simulated. The mask layout is ready to complete according to layout design methodology and rules. After that, we will tape the wafer out in AEMD lab and test the structure parameter comparing with the simulation and correction. And the whole process will be completed.

Acknowledgments

This CMOS baseline work has been supported by 985 Project from the ministry of education. The corresponding author is Xiulan Cheng and any question please contact us.

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