The Design of IP Core for Configurable LCD Controller of MIPI Interface Based on NIOS II

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Abstract. With the LCD controller of MIPI interfacewidely used in portable embedded systems, this paper combines MIPI technology and Altera's NIOS II soft core processorand completes the design of IP core for the LCD controller of MIPI interfacein FPGA. The IP core can be implemented image display with different resolutions without changing the code. After the RTL function level simulation, the LCD controller of MIPI interface can meet the requirements of the LCD controller timing. Experiments show that the IP core can be easily applied to the NIOS II embedded system as the core of various images displayed.

1. Introduction

With the continuous development of science and technology, the LCD display technology for MIPI interfaces becomes more sophisticated.Its outstanding merits have been favored by many industrial and military fields with small volume, light weight, low power consumption, low voltage, high information capacity, easy integration, high reliability and low radiation.

At present, the liquid crystal display is almost all VGA interfacein many industrial and military fieldand it isalready difficult forVGA display interface to meet the needs of industrial and military fieldsto achieve high definitionand small size. Therefore, considering the design of IP Core for the LCD controller of MIPI interface[4], it not only shortens the product development cycle, but also reduces the cost.

In this paper, with reference to other documents on the basis of relevant, we design the IP core for the LCD controllerof MIPI interface based on NIOS II which can be configured to the LCD controller of MIPI interface, which can not only achieve accurate timing under the LCD controllerof MIPI interface of driver functional, but can also be achievedmore standard high-resolution display without changes in the existing code.

2. Working principle and general structure of the LCD controller of MIPI interface

2.1 MIPI profile

MIPI (Industry Processor Interface Mobile)[4] is a consortium established by ARM, Nokia, ST, TI and other companies in 2003. The purpose is to make the interface of the mobile phone such as camera, display interface, radio frequency and baseband interface in order to reduce the complexity of mobile phone design and increase the design flexibility.The advantage is lower power consumption, higher data transmission rate, smaller PCB space[3], and specifically for the optimization of mobile devices, therefore，it is more suitable for mobile phones and smart tablet connection.

2.2 Working principle of the LCD controller

The LCD controller which is based on the SOPC system Avalon bus[4] and the core works need to have a memory to store the display data.After the core software configuration, the memory is not required to participate in the core, and theLCD controller alone operates and takes the initiative to apply for operating the system bus.Display data transmission can be operatedon the basis of the use right of the system.The LCD controller which is an Avalon Bus-Master module is connected to the Avalon bus for display data which is removed from the FIFO memory. Valid data is displayed on LCDscreen,after data, control signals, and clock signals are sent to the LCD screen.

2.3 Overall structure

There is a one to one relationship between the data in the FIFO memory and LCD pixels. The function of the LCD controller of MIPI interface is to transfer the data in the memory FIFO[2] to the LCD screen and complete the display of the LCD screen.In this paper, the design ofthe LCD controllerof MIPI interface has the following several modules: LCD clock module, LCD timing generation module, LCD control module and memory FIFO module. The overall structure of the LCD controller of the MIPI interface is shown in Fig. 1.

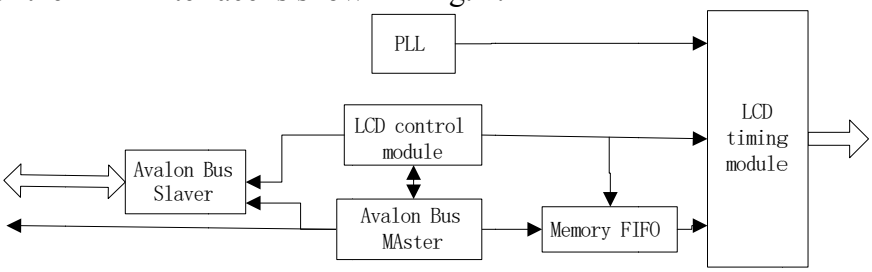

Fig. 1 The overall structure of the LCD controller for the MIPI interface

3. The designof the LCD controllerof MIPI interface

3.1 The design of the LCD clock module

The outside of the crystal oscillator clock which doesn't meet the design of demandis 50MHz.The FPGA internal components of the PLL circuit[1] for frequency multiplication / frequency division NIOS II system generate the required clockNIOS II system clock, the LCD controller display pixel clock and SDRAM clock.The SDRAM clock with theNIOS II clock is set to the same frequency and different phasein order to ensure theNIOS II system stably working. The LCD controller clock can be generated according to the actual needs of different resolutions by settingthe parameterof the PLL as shown in Fig. 2.

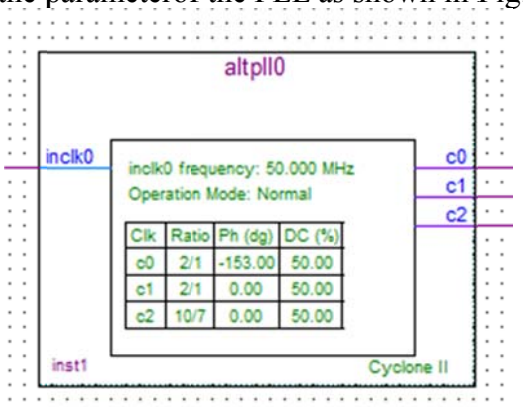

Fig. 2Phase locked loop PLL

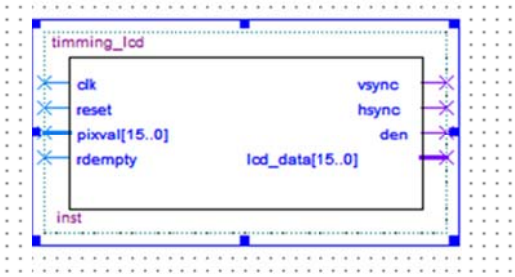

Fig.3 The LCD timing module

3.2 The design of the LCD timing generator module

The main function of the LCD timing generating module is to generate the three synchronous signals[2]: the vertical sync signal,the horizontal sync signaland the data effective signal. According to the timing characteristics of the LCD, it can be known that the counter can be used to implement the circuit of the timing generator, one is the pixel counter, and the other is the counter of the statistical line.When the pixel counter is full line of data, the pixel counterbegins to reset, then counting.When the pixel countsa full line, the line counter is incremented by one.When the line counter is full row, the row counter starts reset. According to the row, the pixel counter and the timing parameters,the synchronous signal vsync, hsync and dencan be generated in the Quartus II generated LCD timing module is shown in Fig. 3.

3.3 The design of Memory FIFO module

Both the working frequency of the LCD controller and NIOS II system are 100MHz, but the display clock of LCD is 74.2MHz.In order to guarantee the stability of the system, two different time domains are added to a FIFO to realize the synchronous transmission of the data in two

different time domains.Schematic diagram of FIFO is shown in Fig.4. In this design,using the Quartus II 11.0 Mega Wizard Manager software comes to generate a capacity of 32 bits * 256 words asynchronous FIFO.

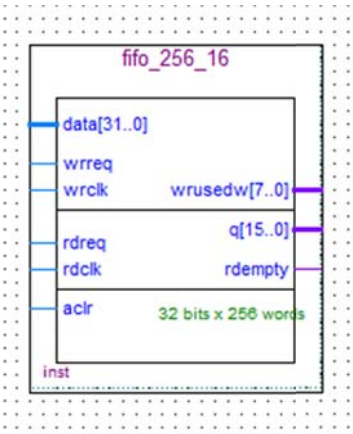

Fig. 4 FIFO schematic diagram

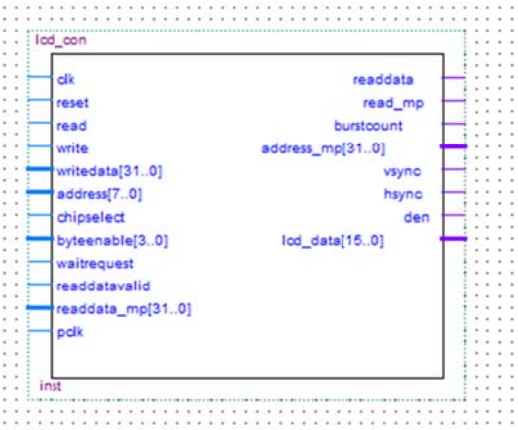

Fig. 5 TheLCD control module

3.4 The design of LCD control module

The LCD control module is used to coordinate the data between the LCD timing module and the FIFO module. In the design of the LCD control module, the port will be based on the FIFO state to launch a burst read and transmission, so the module is an important part of the whole control design.Under normal circumstances, the LCD control module will be empty or full use of FIFO data to determine the use of the logic.Generated theLCD control module is shown in Fig. 5.

4. Simulation and experimental verification of the IP core timing of the LCD controller of MIPI interface

4.1Simulation of IP core timing of the LCD controller

In order to facilitate the simulation, the design of parameter is shown in Fig.6.The IP core is written in Verilog HDL language.Firstly in the Modelsim SE-64 10.0c of RTL function simulation, the simulation results are shown in Fig. 7 and Fig. 8.When the horizontal sync counter is full, the column sync counter pluses 1from Fig. 7, with meeting the demand of the LCD controller timing.

In the process of simulation, the input pixval[15:0] data whichused the code shown in Fig. 9 produced a 16 bit random number.It shows that the output data data[15:0] is the same as the input pixval[15:0] with the enable signal den for one from Fig. 8, which satisfies the needs of data.

```
29 parameter    number_of_columns          =800 ;
30 parameter    number_of_rows             =1280;
31 parameter    horizontal_blank_pixel     =170 ;
32 parameter    horizontal_front_proch_pixel =150 ;
33 parameter    horizontal_sync_pulse_pixel =50  ;
34 parameter    vertical_blank_lines       =150 ;
35 parameter    vertical_front_proch_lines =150 ;
36 parameter    vertical_sync_pulse_lines  =5   ;
```

Fig. 6 The design of the time series parameter

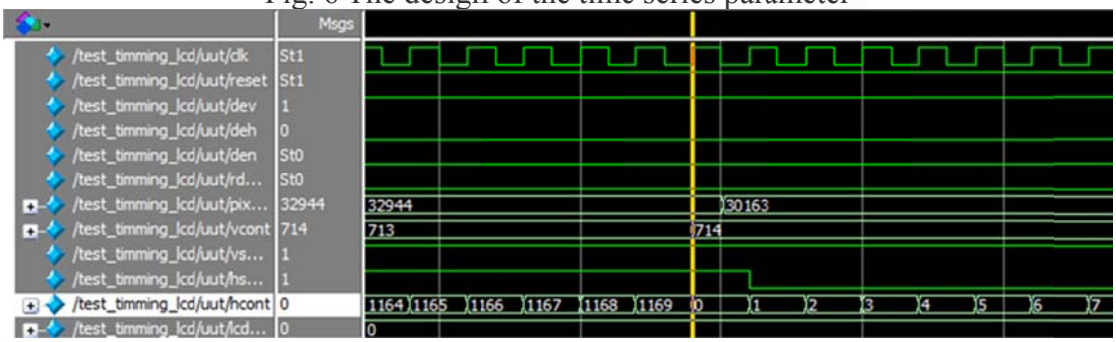

Fig. 7 Simulation results of Modelsim as 1

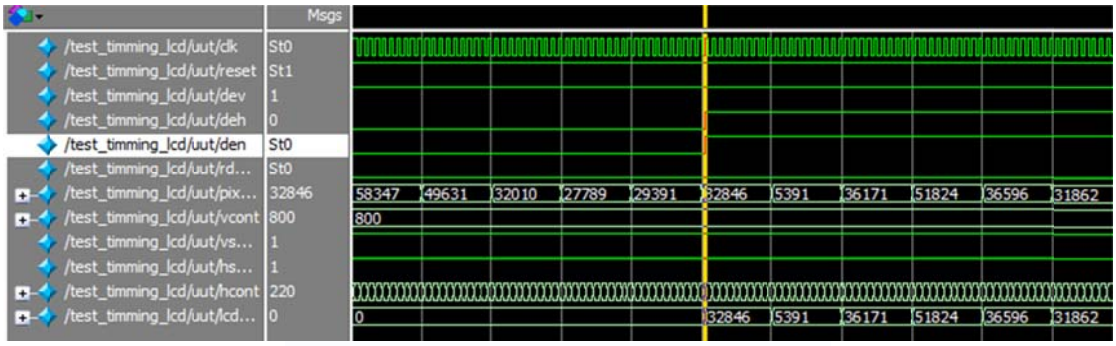

Fig. 8 Simulation results of Modelsim as 2

```
initial begin
    #1;
    //Initial value
    pixval = 16'b0000000000000000;
    forever begin
    #(10*CYCLE);
    //Assignment
    pixval = $random;//Random number
    pixval = pixval%65536;//Randomly generated 65536 numbers
    end
end
```

Figure. 9 16 random generation of binary digits

4.2 Experimental verification

Based on the architecture of the LCD controller ofMIPI interface, it can achieve a higher resolution of MIPI interface phone screenby a simple modification of the time series parameters.This design combines the requirements of TKIS-I helmet type color image sonar project,the mobile phone screenof the size for 5 inch and the resolution for 720*1280, whose parameters are shown in Fig. 10.The experimental results show that the LCD controller for the MIPI interface can be realized by the C language code written in the NIOS II development environment.Fig. 11 shows the display of a sonar image made by the TKIS-I helmet mounted color image sonar.

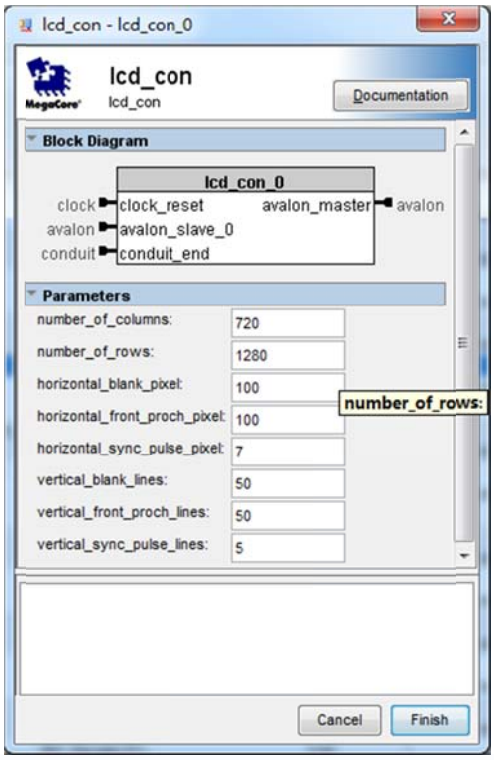

Fig. 10 The design of different frequency LCD time series parameters

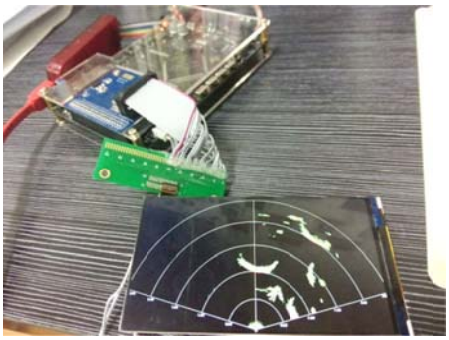

Fig. 11 Experimental results of the project

5. Summary

With the wide application of LCD display in embedded devices, the requirements of the multi resolution display of embedded system are presented.This paper discusses the design of IP core forconfigurable LCD ControllerofMIPI interface.According to the top-down design idea，the function of IP core divided and designed, the timing of IP core simulated and the IP packaged into NIOS II system,whichare well tested by experiment.Since the IP core is configurable, it can be easily applied to the embedded system with NIOS II as the core.

References

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