Analysis on the Ultra-low Power Integrated Circuit Technology

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Abstract. The technology has been integrated into the nanometer scale, the challenges posed by the increasingly obvious power, has gradually become a major problem restricting the development of integrated circuits, as well as the preparation of the core issues and design of integrated circuits exist. Low-power IC implementation is a systematic project, need to consider the power of optimization devices, systems and circuits in a compromise between power and performance process. At present, most of the low-power technology is difficult to address power limitations of IC development fundamentally, which affects the development of nano-scale integrated circuits to a certain extent. Firstly, a simple analysis of the integrated circuit power, further information on the ultra-low power integrated circuit technology, device structure and design.

Introduction

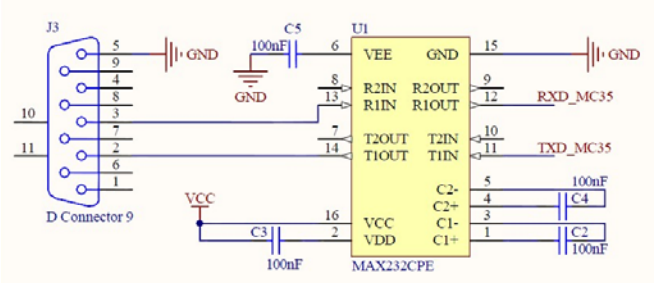
Silicon integrated circuit technology has been rapid development along Moore's Law, according to forecasts this trend can continue at least until 2026, the size of the device will be reduced to 6nm, silicon-based integrated circuit and therefore a longer period of time in the future However, any of the mainstream development of microelectronics technology. With silicon-based integrated circuit technology into the nano-scale, integrated circuit design time, the area is no longer a single objective consideration of the challenges posed by power, integrated circuit development has become a core issue to face. On the one hand the majority of portable battery-powered equipment is used, the power consumption of the integrated circuit determines the time of your device, on the other hand, SoC technology has been developed so that all components integrated into a single chip as possible, but a number of processing units power transfer heat, causing the chip temperature rises, silicon failure, reducing reliability. Power consumption limit has become a major constraint microelectronics technology development.

Power Analysis

Power IC include short-circuit power, static power and dynamic power three parts, namely straight short-circuit power consumption, since the input waveform is not the ideal wave circuit, there is a rising edge and falling edge, so when input In Vtn level to Vdn + Vtp stage, it will lead to a CMOS circuit in NMOS and PMOS transistors are turned on, resulting in short-circuit current, causing a short-circuit power dissipation during switching. Also known as static power leakage power, static power consumption ideally circuit is zero, but in fact is not zero static power consumption, which is due to the presence in the transistor off-state leakage current, causing the static power consumption[1]. Dynamic power is the circuit during switching the load capacitance charging and discharging power consumption. However, the total power consumption of the integrated circuit also involves a lot of factors, such as: operating frequency, supply voltage, transition factor and so on, low-power design should I start from the above factors, in the design of the integrated use of different strategies to eliminate or reduce the above factors the impact on power consumption, achieve better low-power effect.

The Device Structure

Ultra-low oxygen IC implementation should from multiple device structure and circuit design efforts, the conventional mechanism of MOSFET device structure optimization primarily through the material, the device structure optimization and technology and other areas to reduce the leakage current of the device, or to ensure the leakage current improve without changing the device characteristics, reducing the total power consumption of the circuit useless consumption proportion. But for nanoscale MOS devices, the leakage current is a tunnel current mainly comprises an oxide layer, a gate induced drain leakage current, source / drain junction reverse currents and sub-threshold current, etc., as the device size decreases, wants effectively suppressing the short channel effect, improve gate control capability, the thickness of the gate oxide layer on the need to continue the reduction, but thin gate oxide thickness will cause the gate tunneling leakage current is increased, thereby increasing the power consumption, the use of metal gate technology in increase to some extent, the physical thickness of the gate, reducing leakage current [2]. The threshold voltage of the source-drain leakage pressure valve a definite link, GIDL effect and punch-through effect will lead to greater, respectively sub-threshold leakage in case of high pressure and low gate-drain voltage, sub-threshold leakage current increase was primarily due the ability to reduce the gated, using ultra-thin SOI devices, the fence / multi-gate devices as well as dual-gate device can effectively enhance the ability of the bar empty, greatly reduce the pressure source and drain valve leakage, which has become the low-power devices than the nanometer scale One good choice, while the use of high mobility channel material can effectively improve device characteristics. On the other hand, another study points ultra-low power device structure is the use of ultra-low-voltage threshold slope of devices, such as: hanging gate field effect transistor Suichuan, utilizing ultra-steep sub-threshold of this feature, in the ultra-low power consumption of integrated circuits have a very broad application prospects. As shown below:



Low-Power Integrated Circuit Design Technology

Power Gating Technology.

Since the leakage current increases, the static power consumption has become an important part can not be ignored, the static power reduction circuit is to reduce the leakage current, which is the main sub-threshold leakage current leakage current, consider the device from the lower power consumption The threshold voltage should be as large as possible, but from the viewpoint of the circuit operating speed, and hope sub-threshold as low as possible [3]. In order to effectively solve the contradiction between power and speed, has gradually been widely used, based on multi-threshold technique refers to the use of multiple thresholds based on multi-threshold power gating techniques in the design of integrated circuits in the same circuit voltage control sub-threshold current. The impact velocity of the critical path using a low threshold voltage, low threshold module called. At the same time in order to suppress the leakage current, the device will connect high threshold voltage between the module and the power supply, called dormant tube.

Dynamic Threshold Technology.

Reducing the feature size of integrated circuits, circuit power supply voltage is reduced, in order to effectively guarantee the speed devices and circuits, reducing the supply voltage while the threshold voltage needs to be reduced, but the threshold voltage will result in reduced leakage current increased while the noise margin will be affected. Substrate modulation techniques and

dynamic threshold device to ensure the device operating at lower threshold voltage, off threshold voltage is high, thereby effectively contradiction between this power and speed, ultra-low-voltage operation circuit, good compatibility of the technology, in many circuit has been applied.

Ultra-Low Operating Voltage.

Ultra-low operating voltage technology for reducing the power dissipation is a certain benefit, how to get the current drive capability to ensure that one of the problems designers face in the case of low supply voltage. Bootstrap circuit is working under an ultra-low voltage increase circuit speed technology, and has been widely used, it contains a pull and pull-down drive control module bootstrap PMOS and NMOS gates. When the circuit does not work, the bootstrap and control module PMMOS NMOS gate voltage is maintained at 0 and VDD, circuit, control module NMMOS and PMOS gate voltage is set to 2VDD and VDD, effectively increasing the drive current.

Energy Recovery Technology.

Circuit at work, get the energy from the power supply, under normal circumstances these energies can only be used once, the dynamic threshold previously analyzed and ultra-steep sub-threshold and so on are for how to reduce the energy consumption of a single. In order to fully exploit the energy acquired power, measures need to introduce cycle, i.e. energy recovery technology. The use of energy recovery technology, circuits using AC voltage of the clock to control the entire workflow AC voltage on node capacitance fro store energy so as to achieve energy recovery, reducing power consumption.

Conclusions

In summary, the integrated circuit after the nanoscale, low power consumption as the main reason impede the further development of the integrated circuit, the new ultra-steep slope pressure valve device, and dynamic threshold devices such as low-power device structure and technology to certain reduce power extent, but needs further improvement, optimization, new materials, device technology and device structure also need to break through and innovation.

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