Research on a novel Dual-Base Transistor (DUBAT) in 0.5 μm Standard Si-base CMOS Process

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Abstract. A novel Dual-Base Transistor (DUBAT) having a negative-resistance characteristic is presented. This device contains a lateral p-n-p Bipolar-Junction-Transistor (BJT) and a Hybrid-Mode Transistor, and is fabricated on silicon based 0.5μm CMOS process, compatible with the standard CMOS technology as distinct from the traditional DUBAT. The structure of BJT and the Hybrid-Mode Transistor is self-designed to have better current enhancement, didn't use the standard component models provided by the process. The total size of the device is 20.55 μm×6.72 μm. The experimental results demonstrates that the average value of the negative resistance is about -1.04 kΩ, the DUBAT has a low valley current of 20.5970 μA, a high peak current of 1.2576 mA and a peak-to-valley current ratio of 61.06. The I-V characteristic of the device is also discussed in the paper.

Introduction

Negative resistance devices(NDR) are being increasingly used in integrated circuits. Such as oscillator circuits [1], digital logic gates [2] and memory circuits [3]. As a voltage-controlled differential negative resistance semiconductor device, the Dual-Base Transistor (DUBAT) has been researched since 1980 by Chung-Yu Wu and Ching-Yuan Wu [4]. Its theoretical model has been developed by Weilian Guo and Caihong Yu in 1994 [5]. A normal DUBAT is constructed by a p-n-p Bipolar Junction Transisitor (BJT) and a n-p-n BJT [4-6]. The BJTs could be lateral or vertical in substrate and the BUDATs were demonstrated in III-V compound semiconductor, SOI, Si/Ge or BiCMOS process but always can not be compatible with the mainstream CMOS technology[8,9]. As CMOS-compatible means wider application, less process difficulty, higher finished product rate and lower price, the research of CMOS-compatible Si-based NDR attracts more and more designers.

In this paper, a novel DUBAT is designed and fabricated by using of the Si-based standard 0.5 μm CMOS process. In order to reduce the area occupation of the chip, the structure of the novel DUBAT is hand-engineered to be a there-terminals device instead of extracting device models from the standard library. This device contains a lateral p-n-p BJT and a Hybrid-Mode Transistor. A Hybrid-Mode Transistor is essentially a MOSFET whose source and drain diffusions serve as the emitter and the collector of BJT, the region between the source and drain serves as the base of the bipolar device. The gate is typically shorted to the emitter or collector[7]. The Hybrid-Mode Transistor can also be regarded as a BJT with an extra gate between the emitter and collector, and it works in a hybrid mode that involves both MOS and bipolar effects.

The Device Structure

A conventional DUBAT is constructed by a p-n-p BJT and a n-p-n BJT. The p-n-p BJT is worked as the feedback device and the n-p-n BJT is worked as the master device [4-6]. The electrical

equivalent circuit of the device is shown in Fig.1.(a) [5]. There are three terminals of DUBAT named as Base (B), Collector (C) and Emitter (E) marked respectively in Fig.1.(a). The collector and the base of n-p-n BJT are connected to the base and collector of the p-n-p BJT separately. The base-emitter voltage (V_{BE}) of the DUBAT is fixed in a positive bias, the emitter is grounding, the collector-emitter voltage (V_{CE}) is fixed in a changing positive bias. In this article, the n-p-n BJT is displaced by a n-channel depletion MOSFET which is working as a Hybrid-Mode Transisitor.
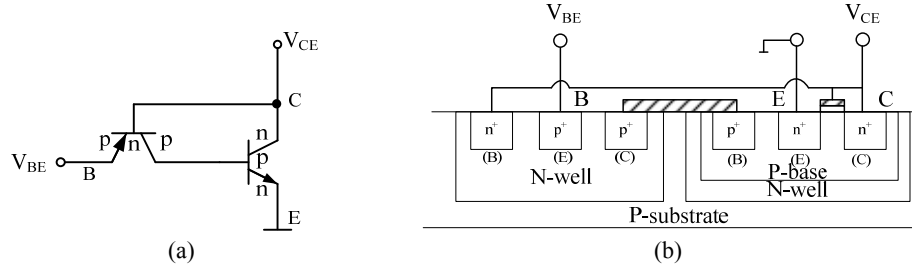

Fig.1 (a) Electrical equivalent circuit of a conventional DUBAT.
(b) The basic device structure of the novel DUBAT

Fig.1.(b) shows the basic structure of the novel DUBAT. There are two N-wells in the P-substrate, and the transistors are grown upon them respectively. The left one is lateral p-n-p BJT and the right one is n-channel depletion MOSFET working as a Hybrid-Mode Transistor. Different from common component models of the standard CMOS process, this n-channel depletion MOSFET is fabricated into a P-base layer which is used as the base region of the transistor.

I_{CE}-V_{CE} Characterizations

The typical I_{CE}-V_{CE} characteristic of DUBAT is shown in Fig.2 [10]. There are five regions in the curve marked as OA, AB, BC, CD, respectively represent the Positive-Resistance Region, the Negative-Resistance Region, the Cut-Off Region and the Breakdown Region. The principle of the negative resistance phenomenon is analyzed as follows.
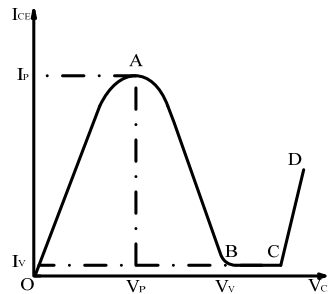

Fig.2. Basic I_{CE}-V_{CE} characteristic of the DUBAT with a fixed negative base voltage drive V_{BE}

A. Positive-Resistance Region: OA

When V_{BE} is fixed in a positive bias, and there is a very small positive voltage on V_{CE}, the gate-source voltage of the MOSFET is positive and is equal to (V_{BE}-V_{CE}). So the inversion channel of the MOSFET is deeper, the drain current of the MOSFET is large. In this case, the forward voltage drop of the emitter-base junction of the p-n-p BJT is equal or less than the drain voltage, so the p-n-p BJT is breakover and operate in saturation with a large base current which is equal to the drain current of the MOSFET. The MOSFET is in linear region.

B. Negative-Resistance Region: AB

As the value of V_{CE} increasing, the gate-source voltage of the MOSFET(equals to V_{BE}-V_{CE}) is redusing，the inversion channel of the Hybrid-Mode Transistor become shallower, the drain current (I_D) which equals to the BJT's base current(I_{B1}) will be reduced. In the end, the BJT operates in the active region. As was shown in Fig.2, I_{CE} decreases when the V_{CE} increases, which makes the I_{CE}/V_{CE} curve AB the first negative-resistance region.

As the Hybrid-Mode Transistor is still in linear region, the collector current I_{CE} could be written as:

$$I_{CE} \cong \beta_F \bar{\mu}_0 C_{ox} \frac{W}{L} \left(V_{BE} - V_T - V_{CE} \right) V_{DS} + I_{CEO1}$$

(1)

C. Cut-Off Region BC and the Breakdown Region: CD

The V_{GS} keeps on reducing , the Hybrid-Mode Transistor will be pinched off. The DUBAT is operating in the Cut-Off Region BC. When the value of V_{CE} is larger than the breakdown voltage of the BJT (BV_{CEO}), the device in breakdown region CD.

Experimental result and analysis

The device microphotograph of the DUBAT is shown in Fig.3. The white dashed block above shows the lateral p-n-p BJT, and the block at the bottom shows the Hybrid-Mode Transistor. The total size of DUBAT is 20.55 μm×6.72 μm.
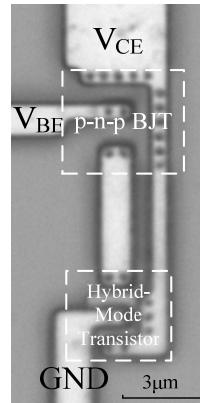

Fig.3. The device microphotograph enlarged 100 times, the total size of the device is 20.55 μm×6.72 μm.

The typical I_{CE}-V_{CE} characteristic of DUBAT is shown in Fig. 4 which was measured by Keithley 4200 at room temperature. As was analyzed before, the input base voltage (V_{BE}) and collector voltage (V_{CE}) are both fixed in positive bias. The V_{CE} is from 0 to 3 V, 0.05 V Per Step; while the V_{BE} is from 0 to 3 V, 0.3 V Per Step. The current peak(I_P) of I_{CE} was observed around 1. 2576mA while V_{BE} is 3V and V_{CE} is 0.8 V.The valley current value (I_V) of I_{CE} was observed around 20.5970 μA while V_{BE} is 3V and V_{CE} is 2V. The valley current is also an important parameter which represent the value of leakage current when the device is off. A 20.5970 μA valley current is small enough for a low power comsumption.
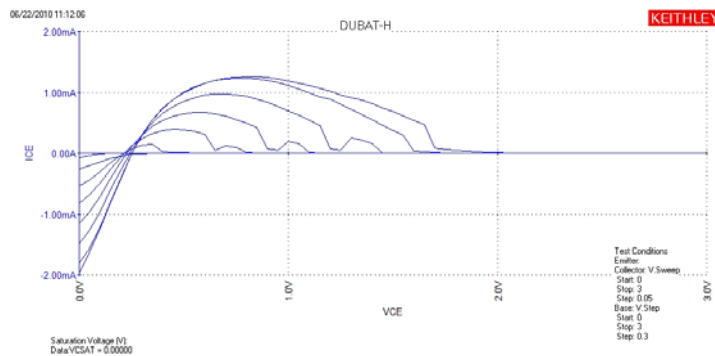

Fig.4. The ICE/VCE characteristic of DUBAT measured by Keithley 4200

The peak-to-valley current ratio (PVCR) is the ratio of I_P divided by the I_V [11]. Therefore the PVCR of the DUBAT is about 61.06.

The negative resistance R_N equals to the derivative of V_{CE} with respect to I_{CE}, i.e. $R_N = dV_{CE}/dI_{CE}$. R_N is negative when the curve is downward. The value of R_N depends on the slope of curve.

The value of negative resistance R_N can also be deduced by the following equations. In Negative-Resistance Region, Equation (1) can be transformed as follow:

$$R_N = \frac{dV_{CE}}{dI_{CE}} \propto \left\{ \beta_F \bar{\mu}_0 C_{ox} \frac{W}{L} \left[(V_{BE} - V_T - 2V_{CE}) \right] \right\}^{-1} , \text{ (as } V_{DS} \approx V_{CE}) \tag{2}$$

Which means, $R_N \propto -V_{CE}^{-1}$, R_N decreases as V_{CE} increases. After calculation that the average value of the negative resistance is about -1.04 kΩ,

Summary

We have designed and fabricated a novel DUBAT in 0.5 μm Standard CMOS Process. The DUBAT is constructed by an n-channel depletion MOSFET and a lateral p-n-p BJT. Both the devices are self-designed to save the chip area, didn't use the standard component models provided by the process. The total size of the device is 20.55 μm×6.72 μm. The DUBAT successfully achieved the negative resistance characteristic with the peak current of 1.2576 mA ,have a very high PVCR as 61.06, and a low valley current as -6.8217 nA. After analysis and calculation, the average value of R_N is about -1.04 kΩ . The DUBAT not only have a efficient new structure and is compatible with CMOS, but also have many good parameters, after further optimization it could be suitable in logic and memory application.

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