Improved Design for Full Wave Rectifier Rectification Circuit

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Abstract. The paper proposes an improved circuit based on peak value hold and compensation sub-circuit. Simulation proves the circuit is suitable to signal in range from 50hz to 1Mhz while keeping low harmonic distortion. The circuit is lower cost than usual circuit.

Introduction

Full wave rectification has wide applications and we can realize our target from it [1,2,3,4]. Any kind of full wave rectification circuit must satisfy low distortion and high accuracy and quick response. The paper [1] has proposed a novel and creative circuit design and comparing to circuit of paper [2,3,4],it has obvious advantage: such as very low distortion and obtaining accurate peak value. It can be illustrated as Figure 1.

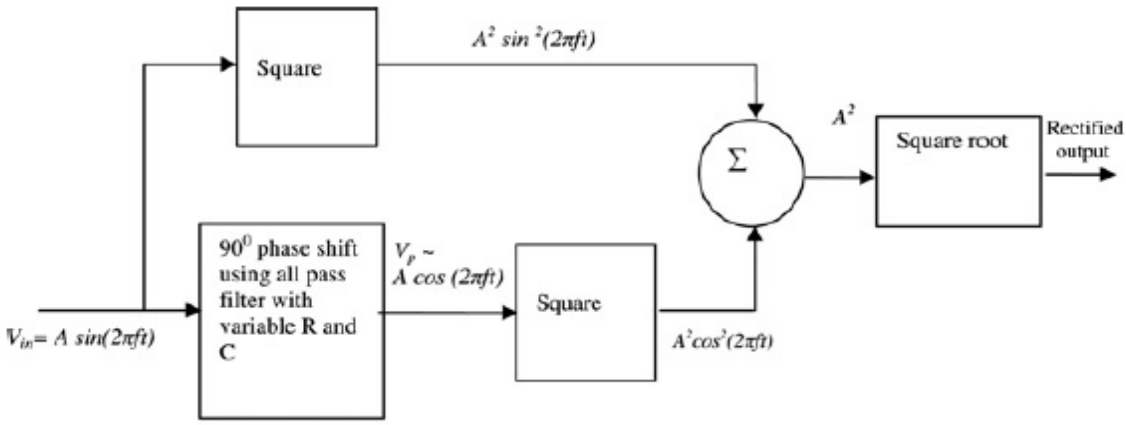

Fig.1 the original design

The typical design for acquiring humidity is as illustrated by Fig.1.

In the application, we find the design in paper [1] can be improved. If the input signal frequency is changed in large range, such from 1Mhz to 10kKhz, the distortion is increased and even equal to circuit in paper [2].The reason causing this is the phase shift circuit and the signal from the phase shift circuit must be equal to 90 degree. The input signal frequency, resistance (R) and capacitor (C) must satisfy formula given below:

$$2pfRC = 1 \tag{1}$$

According to formula (1), when input frequency is 1MHz, we can taken R=159.2Ω and C=0.001uF, the phase shift is equal to 90 degree. But if frequency is down to 10Khz, the phase shift is nearly 0 degree, namely without any phase shift. So the ripple according to paper [1] will be increased and assuming the amplitude of the input signal is noted as Vin, the ripple will reach Vin/2. The measurement result is not useful to us.

Keeping this in view, the paper proposes a kind of circuit and the circuit can keep high accuracy and low distortion in wide frequency range.

Circuit design

The design is illustrated as follow:

By simulation we find out the voltage on the capacity C4 in Fig.1 decreases with the input signal frequency increasing. So the design circuit is added the compensation part to improve the accuracy and the compensation circuit should increase output voltage as input frequency increasing.

In Fig.1, the IC chip 74HC4066 [3,4] is the quad bilateral switches; the function can be described as Figure.2. The pin 5,6,12,13 act as EN function. When the logic level is 1, the switch will be off; when the logic level is 0, the switch will be on. This can be described as Tablet 1. When the switch is on, the signal V3 will pass through the quad switch and appear on the output pins 1,4,8,11. They are paralleled to provide the total output signal.

The EN signal derives from the comparator of LM211, its function can describe as Fig 4. When the positive input is greater than then negative input, the output will be high; otherwise the output will low. So it can control the quad switches. When the 74HC4060 is on, the input signal will charge the capacity C4, until reach the peak of the input signal. When the switch is off, the peak value will hold on the capacity C4. In order to improve the accuracy, namely decreasing the uncharged loss, in this design, choose the LF353N operation amplifier, which input is based on the FET (field effect transistors) construction, and has less input current.

Since the turn-on resistance of the field effect transistors (FET) is controlled by the voltage on gate electrode in ohmic region, so we can change the amplification factor in Fig 1. We employ N channel FET 2N3458 as the variable resistance. The control voltage on the gate electrode is source from the amplifier U2A [5,6,7].

According to the characteristic of operation amplifiers, the output signal of 74HC4066 will equal the voltage of output pin of OPA U1A. The voltage will be enlarged by the following formula:

$$Av = -\frac{R3}{R2} \tag{2}$$

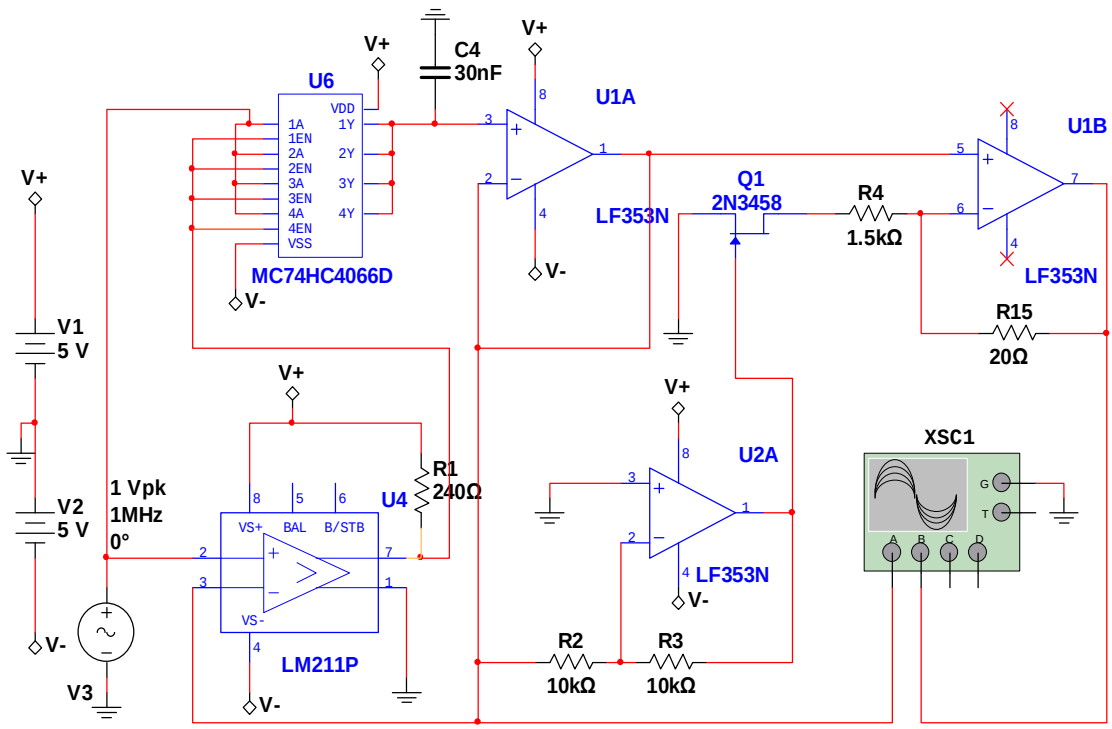

Fig.1 design circuit

In this design, we take R2 equals to R3, the value is 10 KΩ, and the amplification factor is -1. So the amplification factor rates of amplifier U1B is

$$Av = 1 + \frac{R15}{R4 + Ron} \tag{3}$$

In formula [3], Ron is the turn-on resistance of FET 2N3458. Its equal resistance can be described as Fig 3.

According to the characteristics of the 2N3458, Ron increases with the gate electron voltage decreasing. Gate electron voltage is opposite to the peak value from amplifier U1A, so with peak value voltage decreasing [8,9], the Ron will decrease and from formula (3), the voltage amplification factor Av increases as the input signal frequency increasing to compensate the output of amplifier U1B. The output value of U1B is enough and it can be sampled by analogy to digital convector (ADC) or others instrument for future using.

The total amplification factor can express as following:

$$A = -\frac{R3}{R2} * (1 + \frac{R_{15}}{R_4 + R_{on}}) \tag{4}$$

When input signal amplitude increases, the Ron can compensate the output decreasing.

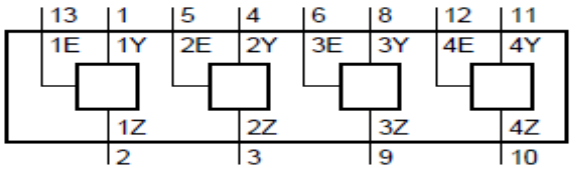

Fig.2 74HC4066 function diagram

Table 1 the truth function of 74HC4066

EN	SWITCH
L	off
H	on

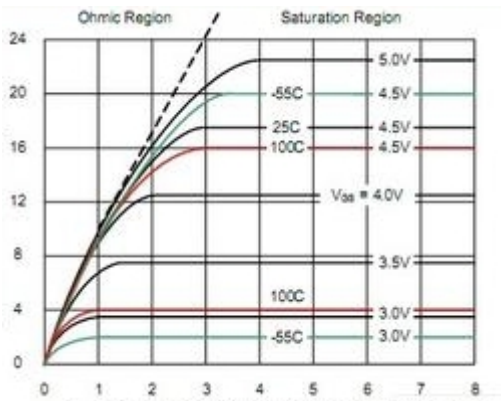

Fig.3 the equal resistance of 2N3458

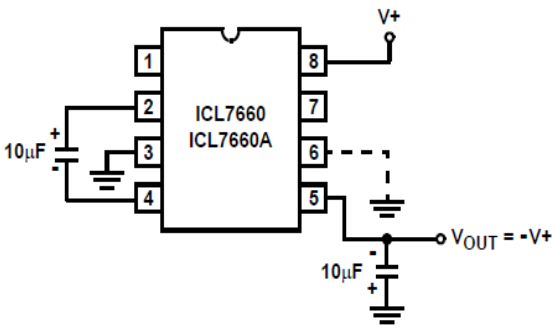

Fig.4 negative voltage circuit

In the Fig.1, the design employ two kind of power source, one provides the positive voltage and the other provides the negative voltage. But in some occasion, there is no negative power source. The design can not work properly.

In such condition, we can employee the IC ISL7660. The application circuit can be described in the Fig.4. When the input voltage is 5V, the output voltage is about -5 volt; this can replace the negative 5 volt power source. The design In Fig.1 can work properly. But this method can not produce very low noise power supply because of its switch working mode. Under very accurate condition, we must add the low noise LDO (low dropout regulator) after ISL7660.

Simulations

By Pspice simulation, we can obtain the output peak value in different input frequency and amplitude. The amplitude can be changed in the Fig.1, the result can be observed by the component XSC1.

From above table 1,2,3, we know the output peak value has a little higher when input amplitude is 0.1V at frequency=50hz, because the compensation point is choose when input amplitude is 1V at frequency=1Mhz.

Table 2 input signal amplitude is 1V

Input signal frequency	50hz	10Khz	500KHz	1Mhz
output voltage	1.016V	1.022V	1.002V	989mV
error	1.6%	2.2%	2%	-1.1%

Table 3 input signal amplitude is 0.5V

Input signal frequency	50hz	10Khz	500Khz	1Mhz
output voltage	0.510V	0.511V	0.504V	0.493V
error	2%	2.2%	0.8%	-1.4%

Table 4 input signal amplitude is 1V 0.1V

Input signal frequency	50hz	10Khz	500k	1Mhz
output voltage	106.2mV	106.1mV	103.4mV	100.7mV
error	6.2%	6.1%	3.4%	0.7%

Conclusion

The paper proposes a kind of design to improve the design.

By simulation we can know the design can be suitable to wide frequency range signal, which lies in 50hz to 1Mhz while keep low harmonic distortion. But with the amplitude decreasing, the error increases, too.

From Fig.1, we know the design does not employee any diode, so the input signal frequency can be enlarged.

According to the price of the chips, the design cost is low. By the simulation, the design can even obtain the peak value of square wave and triangle wave.

If there is not -5V volt power source, we can employee the ISL7660, which can produce negative power supply.

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