

Design and Implementation of IP Core of Interactive Projection Gesture Image

Deng Yaohua^{a*}, Zheng Zhihang^b, Wu Liming^c and Zhang Qiaofen^d

Guangdong University of Technology, Guangzhou 510006, China

^adengyaohua@gdut.edu.cn, ^bzhengzhihang1991@foxmail.com,

^c2801396971@qq.com, ^d1334094259@qq.com

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Abstract. In order to improve the speed of gestures image processing in interactive projection, the paper uses field programmable logic devices to design image processing system on-chip, studies the realization method of image wavelet transform IP core, designs gesture image of Haar wavelet decomposition and reconstruction IP core based on Xilinx FPGA. The experiments show that the effect of gesture image processing using the IP core is consistent with the results of PC processing, the processing time is improved by 4.6313% compared with PC, good foundation is built for subsequent experiments of interactive gesture recognition and matching.

Introduction

Interactive projection is a new type of multimedia display platform that can provide fantasy dynamic interaction experience [1]. Most interactive systems use the video acquisition card to capture gesture images, through computer [2], according to the matching results to implement corresponding functions. However such system's responding speed is slower compared to new device. In this paper, FPGA with high-speed parallel processing mechanism was selected to design interactive system to improve the reaction rate, get fast processing speed, and strong interactive projection image processing SoC.

Design scheme of image processing system on-chip

Overall program

Fig. 1s designed to integrate image acquisition, image processing, projection imaging control multicore SoC chips chart [3]. Its inside consists of 2 32-bit microprocessors soft-core of MicroBlaze, 4 user-defined independent computing IP cores and 6 Xilinx EDK standard IP cores, each IP core directly implements their respective mandates and collaborates with MicroBlaze soft-core processors. An XPS_Mailbox IP core is used to realize synchronization between 2 MicroBlaze processors, connects to bidirectional bus ports. Each port has an interrupt interface, when one port of the processor write data to the message mailbox (Mailbox), the other port will generate an interrupt to notify the other party Mailbox data has been written. The XPS_Mailbox IP core utilize PLB bus interface, realizing

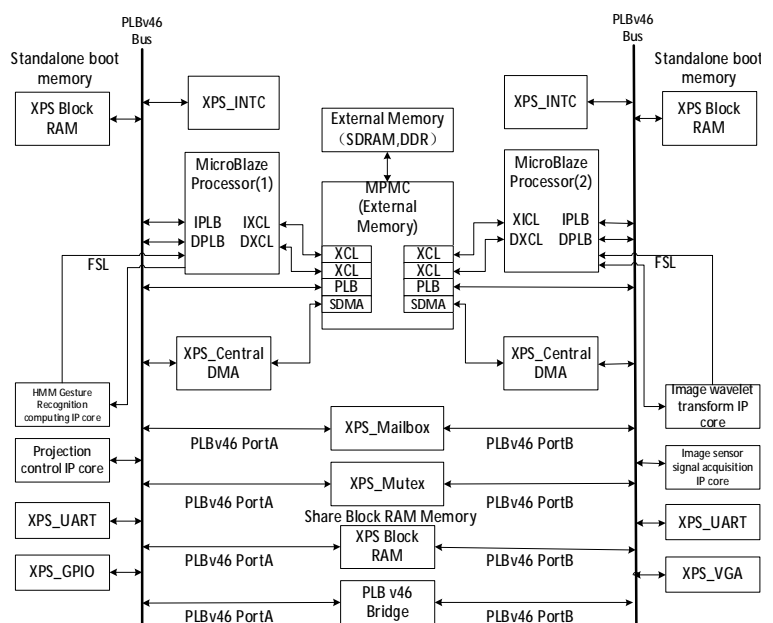


Fig. 1. Multi-core SoC chip architecture diagram

reading and writing functions by `Xmbox_ReadBlocking ()` and `Xmbox_WriteBlocking ()`. Its Mailbox length is 4K and data width is 32 bits.

Fig.2 is the flowchart of image processing. The processing is composed by the following parts. Firstly, analog camera collects and processes image video information; the information enters into image sensor signal acquisition module after it converted to digital video by decoder chip TVP5150. Secondly, conduct wavelet transform of processing image. Thirdly, extract gesture image profile; then making linear fitting and arc fitting. Finally, gesture matching and execute the corresponding action [4].

The segmentation of human body with virtual object image in background.

In case of the front projection imaging, after the camera acquisition picture is an image including

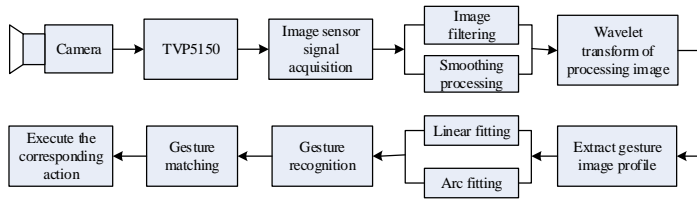
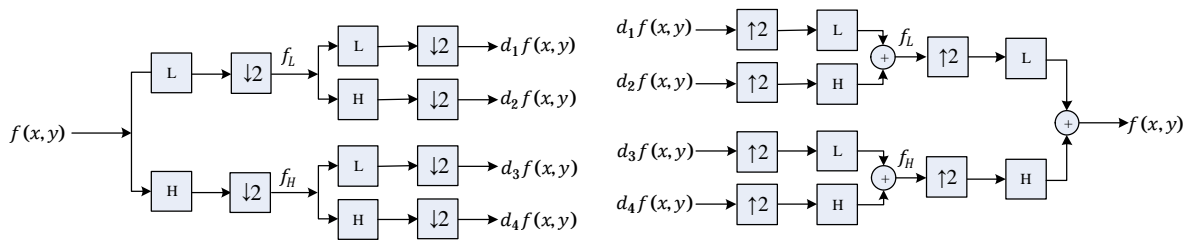


Fig.2 Flow chart of image processing

Fig. 3 Gesture contour characteristic

user gesture, due to the presence of the projection surface is often uneven, flares or shaded area, which will cause acquired projection region boundary is inconsistent with target boundary.

Observation profile characteristics of different gestures (shown in Fig.3. We can find there are contain different numbers and shapes such as line, arc and other geometric elements, when we do multi-scale segmentation of human body with virtual object image in background, the extraction of the geometric elements quality will directly affect success rate of subsequent gesture recognition.



(a) decomposition process

(b) reconstruction process

Fig. 4 Schematic wavelet decomposition and reconstruction process of

If gesture images are defined as $f(x, y)$, then $d_1f(x, y)$ reflects low-frequency components in both the horizontal direction (x) and the vertical direction (y) after conducting the two-dimensional wavelet transform for processing image, $d_2f(x, y)$ reflects the low-frequency components in direction x and high-frequency components in direction y , $d_3f(x, y)$ reflects the high-frequency components in direction x and the low-frequency components in direction y , $d_4f(x, y)$ reflects high-frequency in both directions x, y [5]. L represents the low-pass filter having the impulse response, while H represents the high-pass filter having the impulse response. According to Mallat algorithm, wavelet decomposition and reconstruction of the gesture image (x, y) consists of several levels of high-pass filter H and low-pass filter L. (shown in Fig.4. To implement row and column respectively, the decomposition result diagram was shown in Fig. 5

The experiment and analysis

The construction of the experimental test platform.

Interactive projection image processing system on Xilinx FPGA IP core verification platform physical photo as shown in Fig. 7. Hardware environment: Intel Core Duo processor, the operating frequency of 3.40Hz, memory 4GB, Xilinx VC2VSP30 FPGA development system, a color CCD

camera, a frame rate of 30fps. Software environment: Microsoft Windows 7 operating system, Xilinx ISE10.1, EDK10.1, Modelsim6.5, MATLAB R2007b.

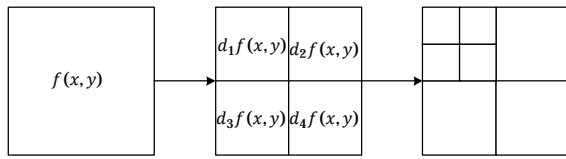


Fig. 5 two-dimensional wavelet decomposition results

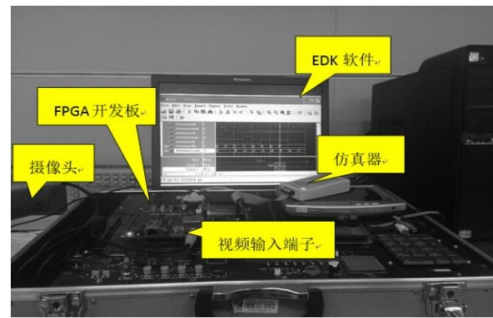


Fig. 6 Xilinx FPGA IP core verification platform

Wavelet decomposition experiment.

Adoption the multi-scale segmentation technology, which analyzed and discussed in preamble. We use a gesture image (shown in Fig.7a) as the test image and choose Haar wavelet as wavelet transform. After the original image to grayscale (shown in Fig.7b)), conduct a two-stage wavelet decomposition, compare image decomposition results of each stage and calculate the consuming time of wavelet decomposition T_{wmtip} .

The whole wavelet decomposition of processing image is divided into 4 stages: the first level wavelet transform in vertical direction result is Fig.7c), the first level wavelet transform in horizontal direction result is Fig.7d), the second level wavelet transform in vertical direction result is Fig.8(e), the second level wavelet transform in horizontal direction result is Fig. 8(f).

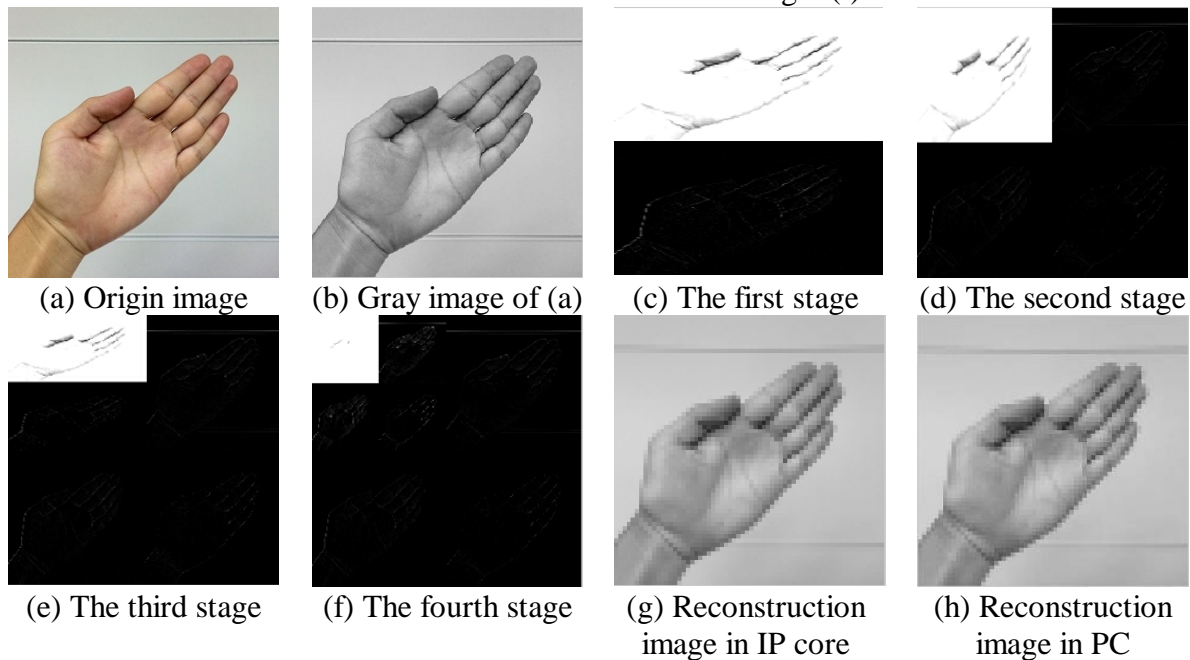


Fig. 7 Secondary wavelet decomposition experiment

From Fig.7c)-(f), we can see that frequency components of gesture image after each stage decomposition relative to wavelet decomposition result of $f(x, y)$ shown in Fig. 4).

Fig.7g) is the processing image after conducting wavelet transform reconstruction; the image is consistent with the result in PC drawing in Fig.8(h). This proves that the correctness of designing image wavelet transform IP core for image decomposition and reconstruction.

In the condition that PLB bus clock cycle is 1×10^{-5} ms, make a test of 10 times about the time required to image wavelet transform hardware IP core decomposition and reconstruction respectively, statistic the consuming time of wavelet decomposition and reconstruction T_{wmdt} , T_{wmrt} and the total consuming time T_{wmtip} , and make a comparison with consuming time T_{wmtpc} in PC.

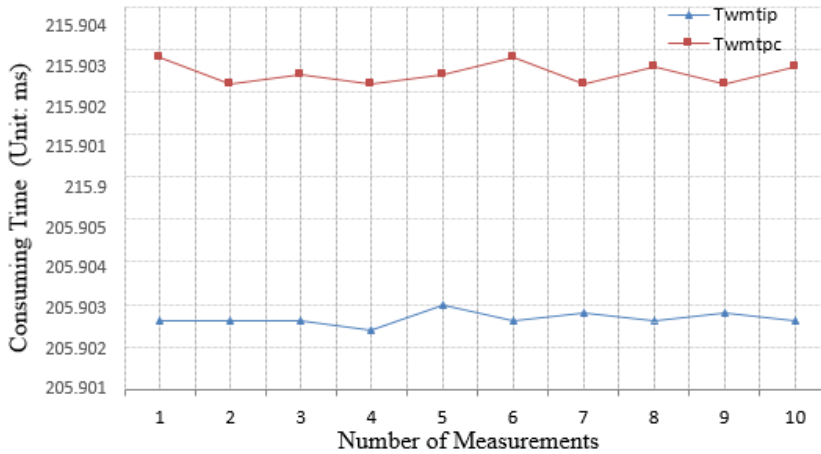


Fig. 8 Wavelet transform in hardware IP core and the PC consuming time comparative graph

Fig.8shows consuming time comparative of wavelet transform in hardware IP core (T_{wmtip}) and the PC (T_{wmtpc}). Further calculations can be obtained: The total consuming time of wavelet decomposition and reconstruction calculated by hardware IP core $T_{wmtip} = T_{wmdt} + T_{wmrt} \approx 205.903ms$ which is 4.631% shorter than $T_{wmtpc} \approx 215.902ms$ the calculated time of PC.

Conclusion

In this paper, image processing hardware IP core design based on wavelet transform was proposed, which is applied to the projected interactive image processing.

(1)Through experiments in the hardware IP core, it was found that effect of processing gesture images by the IP core is consistent with that by PC, obtained a clear gesture outline and an edge shape and other low-level features.

(2)The wavelet transform processing time of gesture image by hardware IP core was improved by 4.6313% compared with PC operation, which building a good foundation for subsequent experiments of interactive gesture recognition and matching.

Acknowledgments

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