The Design of Normally-off 1300V 4H-SiC VJFET

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Abstract: Results are presented for the silicon carbide (SiC) vertical channel junction field effect transistor (VJFET) fabricated based on in-house SiC epitaxial wafer suitable for power devices. The Normally-off 1300V SiC VJFET device's current density is 260 A/cm^2 and current is 8 A at V_G= 7 V and V_D = 2 V, with related specific on-resistance 7.56 mΩ·cm^2. The device exceeds 1300 V at gate bias V_G = 0 V.

Introduction

The power devices are mainly fabricated using silicon as the semiconductor material. Si device design and fabrication technology has matured over the past six decades. 4H-SiC has been shown to have tremendous potential for high power electronic devices. SiC power devices has been a stable segment in the power electronics market in recent years. Like the MOSFET, the implanted VJFET is majority carrier device and has the potential to yield fast switching, high voltage with a low on-resistance. The voltage on the gate modulates the current flow from the drain to source regions. SiC JFET do not exhibit the low channel mobility of the MOSFET and it is thus device for applications in which the normally on characteristic is not a severe disadvantage, for example in a cascode connection with a normally off device such as a Si MOSFET. In many applications, use of normally-on transistors leads to circuit improvement.[1][2]

Previously, we have demonstrated 8.9 mΩ·cm^2, 240 A/cm^2, 5A, 1300V 4H-SiC VJFETs with a vertical-channel structure fabricated in-house [3]. In this article, we report our progress research on DC and experimental results of normally-off 1300V 4H-SiC VJFET. The fabrication process is also described in detail.

Design and Experimental

The epitaxial structure view of a SiC VJFET are shown in Fig. 1. A successful design of the SiC VJFET is shown in Fig. 2. The SiC VJFETs are fabricated on a highly doped n^+ 4° off-axis Si-face 4 inch 4H-SiC substrate with epitaxially grown n^+ buffer, n^- drift, n^- channel, and n^+ ohmic contact layers. The ohmic contact layer is heavily doped to $n^+ = 2 \times 10^{19}$ cm^{-3} for Ni / SiC source ohmic contact formation. The n^- channel layer is 1.6 μm thick and doped to 3×10^{16} cm^{-3}. The drift layer is 12 μm thick and doped to 6×10^{15} cm^{-3}. The n^+ buffer layer is 1 μm thick and doped to 1×10^{18} cm^{-3}. The n^- type channel layer is used to form the vertical channel and the drift layer is designed to block over 1300 V. For VJFETs that require no epitaxial regrowth where gating is provided by implanted vertical p -n junction. The implanted and lift-off trenched gate is formed by ICP etching and Al^+ implantation. The gate of the PN junction type offers wider process latitude, especially with respect to the thermal budget and the function of anti radiation. To obtain the forward current, a positive voltage must be applied to the gate. The maximum gate voltage is limited by the built-in voltage of the junction between the gate p^+ region and the channel layer. The single chip has a total area of 9 mm^2 (3×3 mm^2). Excluding the bonding pads and edge termination regions, the p-n-junction active area is 3 mm^2. Edge termination is provided by a self-aligned floating guard-ring structure, which is p^+

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implanted simultaneously with the gates. The n-source and p-gate regions are simultaneously metallized with Ni with the e-beam evaporation and lift-off processes. The gates and sources Ni ohmic metal layers are annealed at 900 ˚C with n^+ 4H-SiC to form nickel silicide ohmic contacts. Dielectric layers are deposited for isolation, and ICP etching opens windows for thick gold interconnect metallization [4]. A successful 1300V 4H-SiC JFET wafer is shown in Fig. 3.

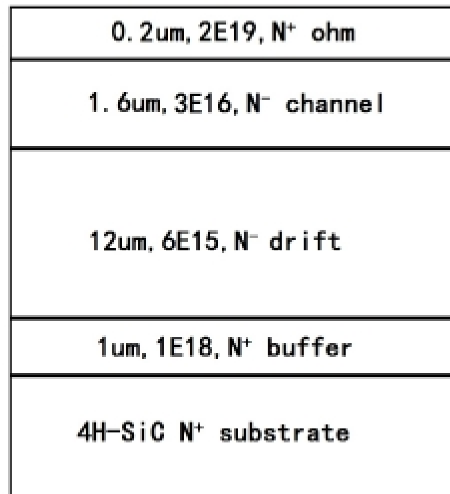

Fig. 1 Cross sectional view of a SiC VJFET

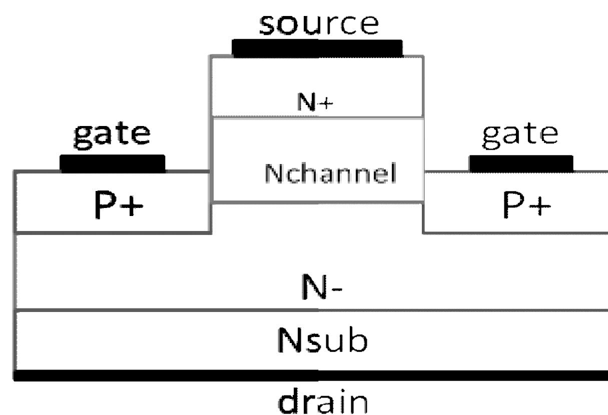

Fig. 2 A designed image of the SiC VJFET

Fig. 3 1300V 4H-SiC JFET wafer

Results and Discussion

The section drawing of 1300 V 4H-SiC JFET device with gate control is shown in. Terminal electric field distributions profile 1300 V 4H-SiC JFET is shown in Fig. 5. Simulated electric field distribution of normally-off 1300V 4H-SiC VJFET using finite element analysis. Optimize the device's structure design through a finite element analysis and adopt 15 terminal protection guard rings according to the results. [5]

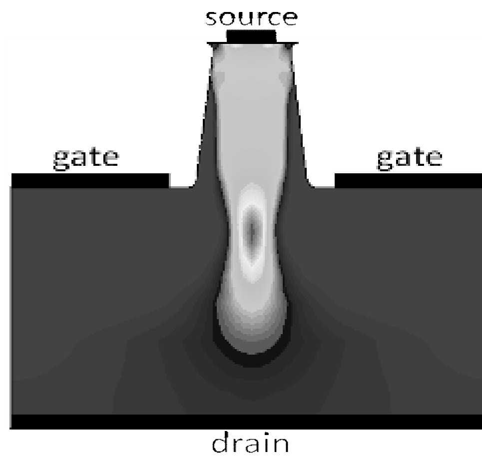

Fig. 4 The section drawing of 1300 V 4H-SiC JFET device with gate control

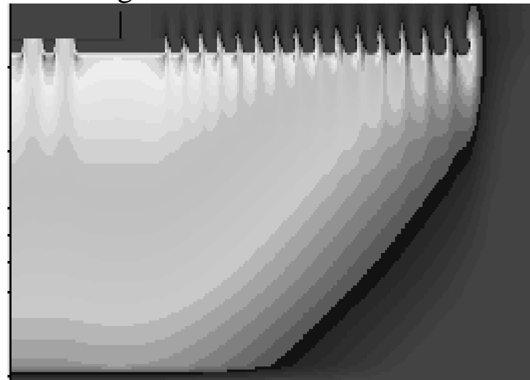
Fig. 5 Terminal electric field distribution profile of 1300 V 4H-SiC JFET

Tektronix 370 is used to measure the devices. From Fig. 6, we can know that the SiC VJFET device yielded a drain current 8 A at a drain voltage of 2 V. The device has a specific on-resistance of 7.56 $m\Omega\cdot cm^2$ not considering the guarding rings area. As illustrated in Fig. 7, the SiC VJFETs' blocking voltage exceeds 1300V at gate bias $V_G = 0$ V with a leakage current equal to 6 μA. The room temperature results are shown in Fig. 6. Because JFET is voltage controlled device without critical gate dielectric functionality, 4H-SiC JFETs are viable high temperature alternatives [6] [7]. More comprehensive test data taken at higher temperatures will be presented later.

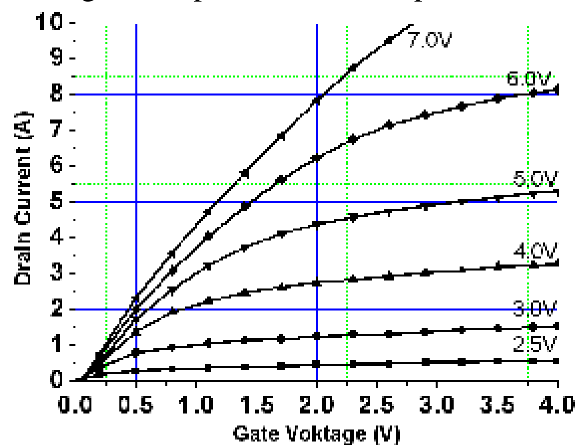

Fig. 6 Forward I-V characteristics up to 8 A with $V_{DS} = 2$ V for SiC VJFET, gate voltage from 2.5 V to 7 V, temperature 25 ˚C.

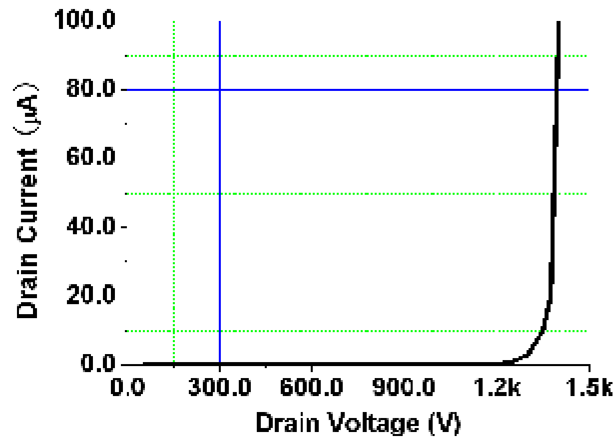

Fig. 7 Reverse voltage up to 1300 V (V_G = 0 V) for SiC VJFET

Conclusion

The capability of the fabricated normally-off 1300V SiC VJFET on n^+ type conductivity 4H-SiC substrates is researched. When V_G is 0 V, the SiC VJFET's reverse blocking voltage exceeds 1300V with a leakage current equal to 10 μA when the temperature is 25 ˚C. The forward drain current is in excess of 8 A at gate bias V_G = 7 V and drain bias V_D = 2 V at room temperature. The SiC VJFET device's current density is 260 A/cm^2 at V_G= 7 V and V_D = 2 V, with related specific on-resistance 7.56 mΩ·cm^2. The existing device structure and fabrication process may be applied to achieve higher blocking voltages, which will require different thickness and doping of the epilayer.

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