Study of Electrical Behavior of Hf-Ti-O Higher-k Dielectric for ETSOI MOSFET Application

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Abstract. The electrical properties of Hf-Ti-O higher-k thin film and ETSOI MOSFET with Hf-Ti-O gate dielectric were studied in this work. To accurately extract the permittivity of the Hf-Ti-O thin film, the different physical thicknesses Hf-Ti-O thin films were fabricated by radio frequency magnetron co-sputtering on Si substrate with SiO_2 interfacial layer. The permittivity of the Hf-Ti-O thin film is 32.5. The MOS device and ETSOI PMOSFET device using Hf-Ti-O higher-k films as gate dielectric were fabricated by atomic layer deposition (ALD). The MOS device shows low equivalent oxide thickness (EOT) of ~0.76 nm, flat-band voltage (V_{fb}) of 90 mV, and gate leakage current density (0.31 A/cm^2@V_{fb}-1 V). And the ETSOI MOSFET with 40 nm gate-length reveals good electric properties with a switch ratio of 2.8×10^4, a high transconductance (Gm) of 2.5 mS, appropriate saturation threshold voltage of -0.158 V and liner threshold voltage of -0.199 V. The drain-induced-barrier lowering (DIBL) of 48 mV/V and a subthreshold swing (SS) of 69 mV/dec indicate that ETSOI PMOSFET has good short-channel control capacity.

1 Introduction

Hafnia (HfO_2) is an important gate dielectric material due to excellent performances with high permittivity (k, 18~20) compare to silicon oxide (SiO_2, k=3.9), high band gap (5.8 eV), large conduction band offset with silicon (~1.5 eV), and good compatibility with traditional substrate material of silicon [1-5]. So far, it has been successfully applied in the 45~22 nm technology nodes [6-8]. With the continued development of CMOS technology, the devices with HfO_2 (k=18~20) gate dielectric are extremely difficult to meet with continued EOT scaling [9]. Considering the other excellent performances of HfO_2, one approach to increase the permittivity of gate dielectric material is combining HfO_2 with other high-k material, namely hafnium-based binary oxide with higher permittivity (k⩾25)[10-14]. Among these higher-k hafnium-based binary oxides, the Hf-Ti-O material is very attractive. The permittivity of Hf-Ti-O can reach 30~50 [15-17] due to the high k (50~80) of TiO_2 [18, 19].

However, TiO_2 has potential disadvantages such as lack of thermally stable with Si or SiO_2 and small conduction band offset with silicon (~1.2eV)[20, 21]. These potential disadvantages will increase the leakage current and worsen the electrical properties of MOSFET device. So the MOSFET device with Hf-Ti-O gate dielectric should be studied extensively. At present, the investigations of the MOSFET devices utilizing Hf-Ti-O higher-k thin film as gate dielectric are rarely and mainly focus on the devices with large gate length [16, 17, 22, 23]. The characteristics (such as threshold voltage, short-channel control capacity) of this device with small gate length are still unknown.

In this paper, the extremely thin silicon-on-insulator (ETSOI) instead of traditional bulk Si is used to fabricate MOSFET device [24, 25]. An Hf-Ti-O material was fabricated to satisfy the requirement of higher k (k⩾25). Then we investigated the capacitance and leakage of MOS devices with small EOT (⩽0.8nm). At last, we investigated the electrical characteristics and short-channel control capacity of ETSOI pMOSFET devices with 40 nm gate length.

2 Experiment

In this experiment, the Hf-Ti-O thin films were fabricated to extract permittivity on (100)-oriented P-type Si wafer with SiO_2 interfacial layer by radio frequency magnetron co-sputtering using pure ceramic HfO_2 (99.999%) and metal Ti (99.999%) targets. This SiO_2 interfacial layer was gotten by ozone oxidization of Si. The physical thicknesses of Hf-Ti-O higher-k thin films were controlled by the sputtering time (3~15 min). Pt top electrode and Al bottom electrode were deposited by sputtering.

The Hf-Ti-O higher-k thin films as gate dielectric in MOS and ETSOI MOSFET were fabricated by ALD. The Hf-Ti-O thin films were fabricated on (100)-oriented P-type Si wafer with SiO_2 interfacial layer (~0.57 nm) by ALD using $[(CH_3)\ (C_2H_5)]_4Hf$, $TiCl_4$ as the metal precursor and deionized water as an oxidant. The component of Hf-Ti-O film was adjusted by metal precursors' cycle index. And Hf-Ti-O films were further treated by a post deposition annealing (PDA) in N_2/O_2 at 450 °C for 15 s. The gate electrode TiN film and capping layer metal W were deposited by ALD. Metal Al bottom electrode was deposited by sputtering. Finally a sintering was carried out at 400 °C in N_2 /H_2 gas for 20~30 min. The ETSOI pMOSFETs were fabricated on SOI wafers by the gate last process [26]. And the preparation of interfacial layer and gate structure is same as that in MOS. The gate length is 40 nm and the gate width is 3 μm.

The chemical composition of HfTiO thin films was investigated by X-ray photoelectron spectroscopy (XPS) using ESCALAB 250. The cross section of HfTiO/SiO_2/Si stack was investigated by high-resolution transmission electron microscopy (HRTEM). Capacitance-Voltage (C-V), current-Voltage (I-V) and

drain current- gate voltage (I_{ds}-V_{gs}) measurements were performed in a probe station using keithley 4200 SCS.

3 Results and discussion

Initially, the Hf-Ti-O thin films were fabricated by sputtering to accurately extract their permittivity. The deposition time is 3 min, 6 min, 9 min, 12 min, and 15 min, respectively. From the HRTEM and XPS analysis (not shown), the deposition rate of Hf-Ti-O films are about 0.85 nm/min, the SiO_2 interfacial layers are 3.4 nm and the Ti content of Hf-Ti-O thin films is 9.1%.

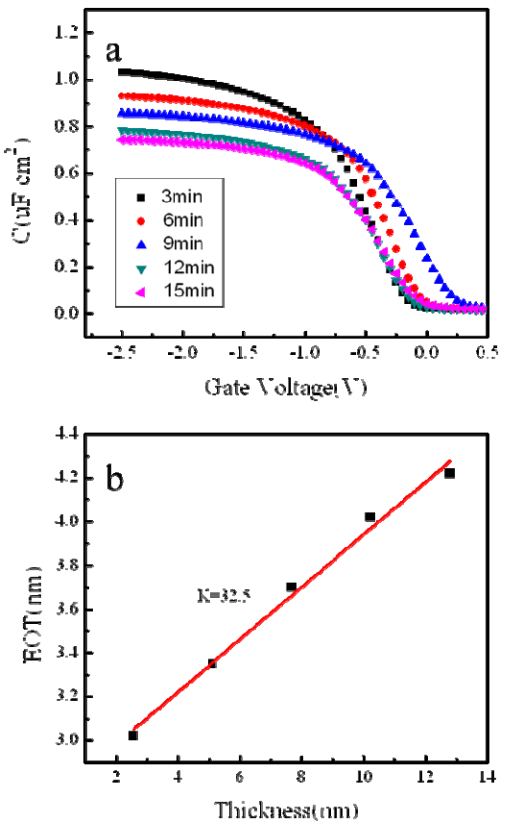

Figure 1. (a)High-frequency (1MHz) capacitance-voltage (C-V) curves of Pt/ Hf-Ti-O/SiO_2/Si MOS device with different Hf-Ti-O deposition time; (b) the value of EOT vs the Hf-Ti-O physical thickness. The permittivity of Hf-Ti-O thin film is 32.5.

Fig. 1a shows the high frequency (f=1 MHz) capacitance-voltage (C-V) curves of Pt/ Hf-Ti-O/SiO_2/Si MOS devices with different Hf-Ti-O deposition time. The EOT of these MOS devices can be extracted from the simulation program considering quantum effect [27]. The value of EOT is linear increasing with the Hf-Ti-O thin film deposition time. And we can plot the value of EOT vs the Hf-Ti-O physical thickness, as Fig. 1b. From the EOT- thickness curve, the Hf-Ti-O thin film exhibits a high permittivity value of 32.5. From Fig. 1, the value of V_{fb} is uncontrollable and the intercept of EOT- thickness curve is 2.74 nm small than physics thickness of interfacial layer. The main reasons are that the high energy atomic beam damages the film and its metal atoms (Hf, Ti) diffuse into interfacial layer to form high k (>3.9) silicate. To get the good quality thin film and interfacial layer, the Hf-Ti-O films of the MOS device and MOSFET devices are fabricated by ALD.

The physics thickness of Hf-Ti-O thin film of W/TiN/Hf-Ti-O/SiO_2/Si MOS devices is 2. 75 nm and the interfacial layer is 0.57 nm. The Ti content is 9.1%, same to the Hf-Ti-O thin film by sputtering.

The capacitance-voltage (C-V) curves of W/TiN/Hf-Ti-O/SiO_2/Si MOS devices were investigated at 1 MHz, as Fig. 2. The capacitance was recorded during double bias sweep, from accumulation to inversion and back to accumulation. From the C-V curves, we can get the characteristics of this MOS device with EOT of 0.76 nm, V_{fb} of 90 mV and without hysteresis. The ΔV_{fb} (~0 mV) indicates these Hf-Ti-O films have good property and few defects.

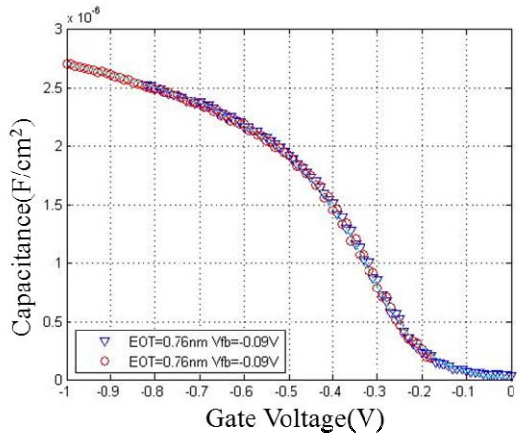

Figure 2. High-frequency (1 MHz) capacitance-voltage (C-V) curves of W/TiN/ Hf-Ti-O/SiO_2/Si MOS device.

Fig.3a shows the gate leakage current density of W/TiN/Hf-Ti-O/SiO_2/Si MOS device as a function of gate voltage (-1.5 V~ 1.5 V). The gate leakage current density is 0.31 A/cm^2 at V_g=V_{fb}-1 V. The gate leakage current density of MOS device with ultrathin gate dielectric is still tolerable for COMS application. The thin SiO_2 interfacial layer and the films with few defects effectively control the gate leakage current density.

Meanwhile the leakage current conduction behavior is studied. The main conduction mechanisms are Fowler-Nordheim tunneling and trap assisted tunneling for relatively high electric field [28, 29]. Fowler-Nordheim tunneling is an electric field assisted tunneling mechanism, but the trap assisted tunneling is related with the film defect trap. At gate voltage rang of -0.8 V to -1.5 V, the ln (J/V_g^2) ~ $1/V_g$ is linear relation, meeting with Fowler-Nordheim tunneling mechanism. The Hf-Ti-O gate dielectric and interfacial layer are rather thin, namely a high electric field. It also indicates the MOS device with few defects.

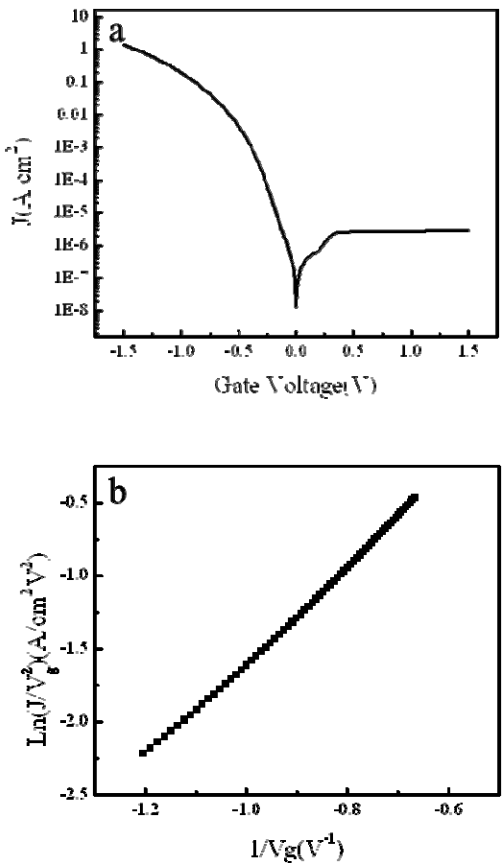

Figure 3. (a) The gate leakage current density versus gate voltage curve and (b) F-N tunneling current curve at gate voltage (-0.8 V~-1.5 V) of W/TiN/ Hf-Ti-O/SiO_2/Si MOS device.

According to the above analysis, the W/TiN/Hf-Ti-O/SiO_2/Si MOS device has good properties with high capacitance density, small EOT, appropriate gate current density and V_{fb}. Next we use the same interfacial layer and gate structure to fabricate the ETSOI pMOSFET device by the gate last process.

The drain current (I_{ds}) measurements were carried out at gate voltage (V_{gs}) range of 0.3 V to -1.3 V, V_{ds}=-0.05 V or -0.9 V (show in fig.4). From the I_{ds}-V_{gs} curves, we can get an off state current （I_{off} =4.85×10^{-8} A@ Vg=0 V) and an on state current（I_{on} =1.38×10^{-3} A @ Vg=-0.9 V) at V_{ds}= -0.9 V. And the switch ratio I_{on}/I_{off} is 2.84×10^4. The ETSOI pMOSFET device has good threshold voltage (-0.158 V @ Vds=-0.9 V, and -0.199 V @ Vds=-0.05 V) and small DIBL (48 mV/V). The low DIBL indicates the ETSOI pMOSFET device have superior short-channel control capacity.

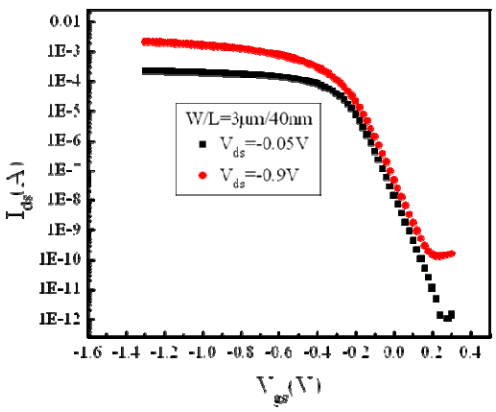

Figure 4. Typical transfer characteristic curve (I_{ds}-V_{gs}) of ETSOI p-MOSFET utilizing Hf-Ti-O higher-k thin film as gate dielectric. The V_{ds} is -0.05 V and -0.9 V.

Fig.5 shows the Subthreshold Swing (SS) and transconductance (Gm) versus gate voltage (Vg) curves of the ETSOI pMOSFET. The low subthreshold swings (69 mV/dec) is achieved at V_{ds}=-0.9 V, indicating excellent interface quality. And the high peak Gm is 2.5 mS at V_{gs}=-0.58 V, which also shows good performance.

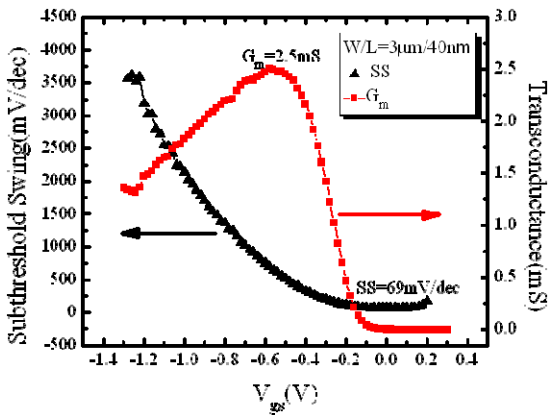

Figure 5. Subthreshold Swing (SS) and transconductance (Gm) versus gate voltage curve of ETSOI p-MOSFET with Hf-Ti-O high-k thin film as gate dielectric.

4 Conclusions

In summary, we studied the electrical characteristics of Hf-Ti-O higher-k gate dielectric for ETSOI MOSFET application. This Hf-Ti-O with a Ti/(Ti+Hf) ratio of 9.1% has a high permittivity of 32.5. Also a low EOT of 0.76 nm, flat-band voltage of 90 mV, ΔV_{fb} of ~0 mV and acceptable gate current density are achieved for the MOS capacitor using Hf-Ti-O thin film as gate dielectric. And the ETSOI MOSFET with 40nm gate-length using Hf-Ti-O higher-k gate dielectric reveals excellent performances with high I_{on}/I_{off} ratio of 2.84×10^4, high peak Gm of 2.5 mS, acceptable saturation threshold voltage of -0.158 V and liner threshold voltage of -0.199 V. Particularly,

ETSOI pFET has superior short-channel control capacity with DIBL of 48 mV/V and SS of 69 mV/dec.

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