Design 8 Bit Analog Unit ADC Integrating Type Single Slope For Low Frequency Application

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***Abstract*—The main component of Analog to Digital Converter (ADC) Single Slope type is an Analog Unit. The analog unit is designed precisely to meet characteristics of the ADC. The ADC design has a resolution of 8 bits and frequency clock of 1 MHz . Openloop amplification of OpAmp is 66.42 dB. Set point voltage comparator at the level of 1.65 V. The value of RC in the circuit integrator = 16µ. The reference voltage used is 2 volts, so that the LSB value obtained is 0,125V. Sample and hold level is designed for 1 µs with a 31.25ns pulse width, resulting in a single enumeration there will be pulse of 16 x 62.5 ns clock. Method of research is done by simulation using mentor graphic with 0,35µ AMS technology. The result is an analog unit design of Single-Slope ADC with a speed of 1 us and maximum of reference voltage is 2 Volt and it is able to give amplitudes sampling up to 0.02 Volt**

Keywords-ramp; ADC; op amps; sampling; integrator

I. ARCHITECTURE OF SINGLE SLOPE ADC [2 , 10]

The main component of ADC Single Slope is a circuit of Integrator. Less precise calculation of the component value determination will result in a significant error in the output, so that it needs as possible minimal percentage of error in the design. The block diagram of ADC circuit is shown in the figure below.

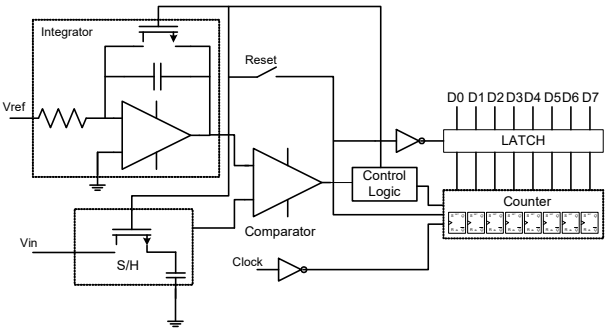

FIGURE I. BLOCK DIAGRAM 8 BIT ADC

The first set is that circuit will be given a sampling voltage for 1 us to reset the counter, latch and begin to activate the switch integrator and S/H. At the same time, the S/H will capture 1 V for the input signal. In sequence, the voltage of integrator starts to rise up to the level of Vref. When the value of Vin is equal to V integrator, the comparator will close or 0 logic. At that time, the clock will be enumerated as many as 2^N times and the result in the latch. Output of D0 – D7 will show the binary value of the input level captured by S/H [1] .

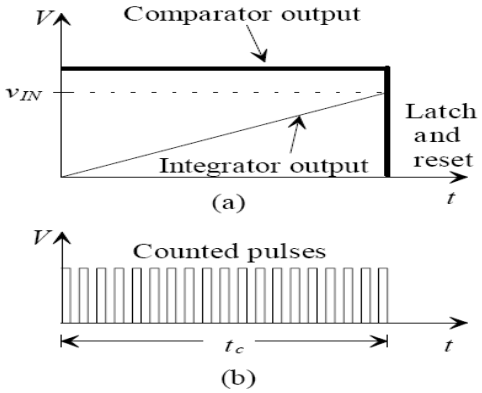

FIGURE II. OUTPUT OF THE COMPARATOR (a). LANCH POSITION OF VIN (b). 2N CLOCK

A. *Transconductance of CMOSOp-Amp(OTA)*

The function of op-amp in the ADC Single Slope is used in the process sample and hold (SHA). Requirements and specifications of op-amp on the ADC [6.7] :

- Open Loop Gain (AoL) $\geq 2^{N+2}$ V/V.
- Open Loop Gain (dB) $\geq$ 20.Log 2^{N+2} V/V.
- Close Loop Gain (AcL) = 2 V/V
- Frequency Unity (fu) $\geq$ 0,22(N + 1) $f$clock.

Figure 3 is a circuit of op-amp OTA. Differential amplifier (M1-4) provides two inputs, inverting and non inverting, that cause noise and offset. High amplification (high gain of M6-7) is almost similar to the not gate when op-amp moves the low load, followed by a buffer stage, common flow (IM5) is provided by the current mirror circuit.

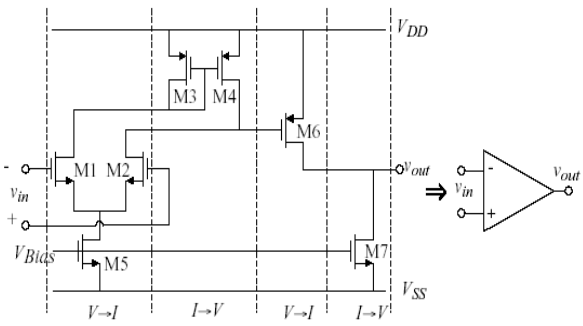

FIGURE III. DESIGN OF OPAMP CIRCUIT

Ideal op-amp has characteristics, such asinfinite open-mode amplification (AoL=~), closed mode aplification (Buffer = AcL) = 1, infinite input impedance (R_{IN}=~Ω), output impedance nearly equal to 0 ($R_o \approx 0\ \Omega$), bandwidth amplification (GBW=~), amount of Vout = $A_V(V_+-V-)$, with Av designed in the open mode amplification (AoL).

All op-amp has a limit on its operation voltage range performance, the limitof CMIR (common mode input range) is the range scale limit of each op-amp input, beyond this limit,it causes output distortion or truncated [3,4,8] .

$$CMR^- = V_{SS} + \sqrt{\frac{I_{D5}}{\beta_1}} + V_{in(\max)} + V_{DS5(sat)} \geq 90\%.V_{OS}$$

$$CMR^+ = V_{DD} - \sqrt{\frac{I_{D5}}{\beta_3}} - \left|V_{TO3}\right|_{(\max)} + V_{in(\min)} \leq 90\%.V_{OS}$$

Function of the current mirror as the bias current source for the MOS component, namely as the controller or activator of the source current toward the control current , for instance Iref = Iout. In figure 3, transconductance stage of op-amp 2 can be analyzed as follows.

$I_{D1} = I_{D2} =$

slew rate (SR) = $I_{SS} = I_{D5}$, $I_{D3}=I_{D4}$,

Amplification of Stage 1

$$AV1 = \frac{gm1,2}{gds2 + gds4} = \frac{2gm1,2}{Iss(\lambda 2 + \lambda 4)}$$

Amplificationof Stage 2

$$AV2 = \frac{gm6}{gds6 + gds7} = \frac{gm6}{I_{D6}(\lambda 6 + \lambda 7)}$$

In which

gds = parameter of transconductance drain to source

λ = parameter of chanel length modulation

B. Function of Comparator [6]

Function of comparator as the comparator of input signal with the reference voltage (ADC), the output of the comparator is 0 or 1 binary logic. In figure 4, it is given a block diagram of precious comparator. In a pre-amp unit, the differential amplifier is used. A decision unit is the heart of the comparator which functions to invert the current to voltage, and functions as a positive feedback by adding the common component. It is used to shift the hysteresis level and also suppress noise. A buffer unit functions as an intermediary of voltage level to binary logic (0.1) .

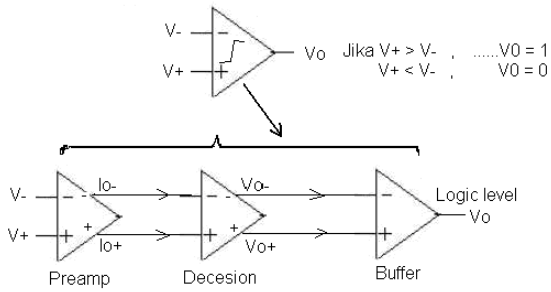

FIGURE IV. A BLOCK DIAGRAM OF PRECISSION COMPARATOR

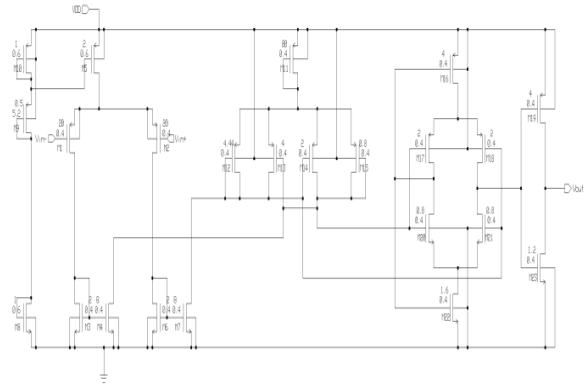

FIGURE V. CIRCUIT OF PRECISSION COMPARATOR

Decision unit functions to change the current level to the voltage level, then the amount of the output voltage depends on the size of M7-M10, and M11 functions as a slider of the hysteresis or to eliminate the noise.

If Io+ is more than Io-, M7 andM9 are in ON condition, M8 and M10 are in OFF condition, if β7 = β10 = β_A and β8 = β9 = β_B and Vo-=0, then:

$$Vo+ = \sqrt{\frac{2Io+}{\beta_A}} + V_{THN}$$

$$Io- = \frac{\beta_B}{2} + \left(V_{o+} - V_{THN}\right)^2 = \frac{\beta_B}{\beta_A} Io+$$

Voltage of switching (V_{SPH}) :

$$V_{SPH} = V_{o+} - V_{o-} = \frac{Iss}{gm} . \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \; for \beta_B \geq \beta_A$$

C. Circuit of Sample and Hold

Unit of Sample and hold is a circuit of CMOS switch with a capacitor. It functions to stabilize the voltage, when sampling is done, where the switch is off and the voltage does not become 0 but is maintained by the capacitor so that the amount is constant when sampling is done [9].

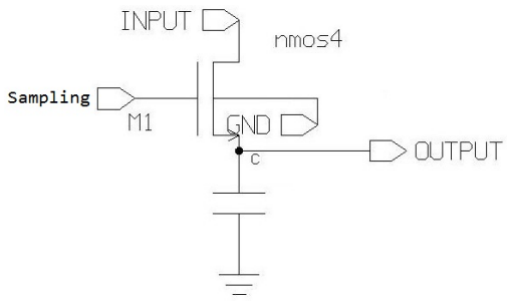

FIGURE VI. S/H CIRCUIT

The amount of capacitor needed is equal tothe amount of capacitor used in the circuit ofLSB capacitor switch, that is equal to 1 pF. For the frequency of 1 MHz, then the amount of resistance is:

$$X_C = \qquad \approx 12{,}9\ k\Omega$$

Amount of impedance of theNMOSswitch when active (Ron) must be much smaller than amount of impedance ofthe Xc capacitor then the value of Ron << Xc, e.i.:

$$Ron = \qquad = 44{,}6\ \text{Ohm}.$$

D. Circuit of Integrator [1,5]

From figure 2a, can be seen that the voltage of integrator (Vc) will rise linearly in accordance with the equation:

$$Vc =$$

$$Vc =$$

When the value of Vc is equal to Vin, the comparator will close and the data will be in the latch. At that moment, the clock will enumerate according to the equation :

$$t_c = \qquad T_{CLK}$$

Since V_{LSB} is equal to then the equation above can be rewritten:

$$t_c = \qquad 2^N.T_{CLK}$$

By referring to the equation 1, the value Vc can be determined again as follows

$$Vc = V_c = \frac{Vin}{RC.f_{CLK}} 2^N$$

N is the value of bits used by ADC to indicate the amount of the resolution. The more the value of N, the better the resolution of ADC.

II. SIMULATION AND DISCUSSION

The ADC architecture consists of the integratorunit, thecomparator and thecounter. In the analog unit, the circuit consists of the integrator, the sample and hold and the comparator .

The main component of the integrator is the OpAmp. The OpAmp simulation resultis shown at the figure below :

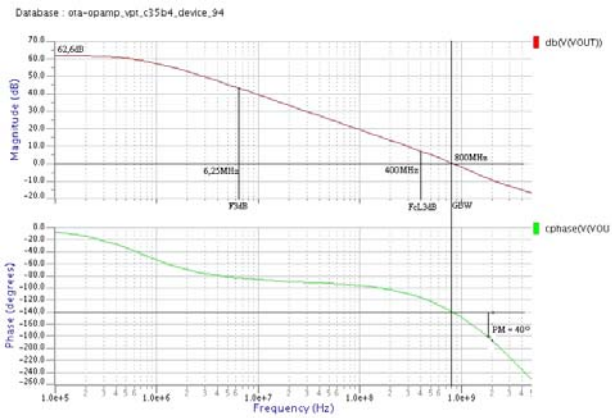

FIGURE VII. OPAMP SIMULATION RESULT

$$AV1 = \frac{gm1,2}{gds2 + gds4} = \frac{gm1,2}{I_{D2}\left(\lambda 2 + \lambda 4\right)}$$

$AV1$= 100,35V/V

$$AV2 = \frac{gm6}{gds6 + gds7} = \frac{gm6}{I_{D6}\left(\lambda 6 + \lambda 7\right)}$$

$AV2$ = 20.89V/V

AV = 2096,31V/V ≈ 66,42dB.

By giving sine input wave of 100KHz and amplitude of 20mV is obtained an output form that approaches the calculation of Vout = 2V .

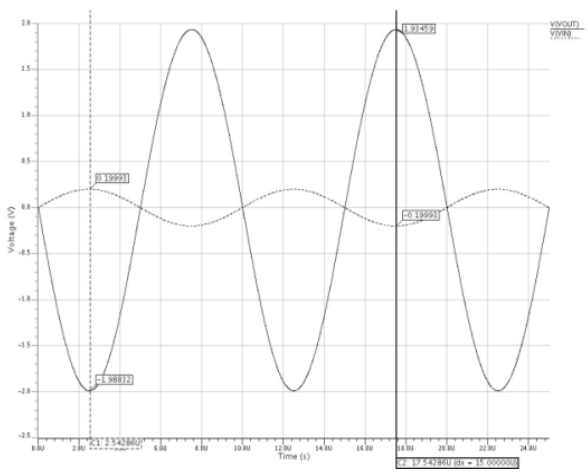

FIGURE VIII. TRANSIENT OPAMP WITH SINEINPUT

In the precious comparator unit (ADC), the simulation is emphasized on the offset of the comparator and the level of the hysteresis to suppress the noise. The simulation result of the testing is.

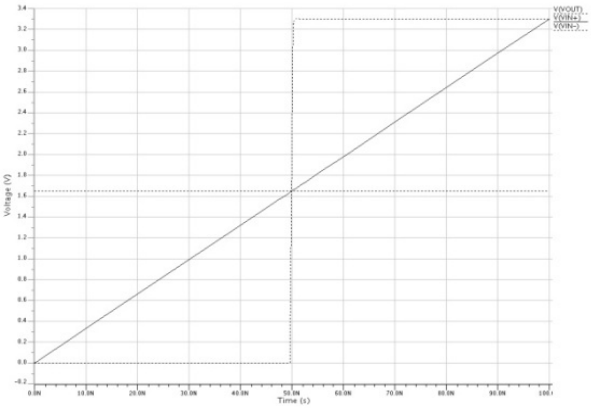

FIGURE IX. SIMULATION RESULT OF OFFSET VOLTAGE

By giving input of Vin- with DC voltage of 1.65V and input of Vin +, variable of DC from 0V to 3.3V, is obtained a change in output (vout) with the set point at 1.65V. When Vin 0V until 1.65V, Vout = 0V (0). When Vin moves from 1.65 V until 3.3V, then Vout = 3.3V.

With resolution of 8-bit ADC by a clock frequency of 1 MHz, value of RC=256µ is earned from the integrator circuit. For the value of R = 100 K, the value of C = 256 pf .

The circuit simulation result of the integrator is shown in figure 10.

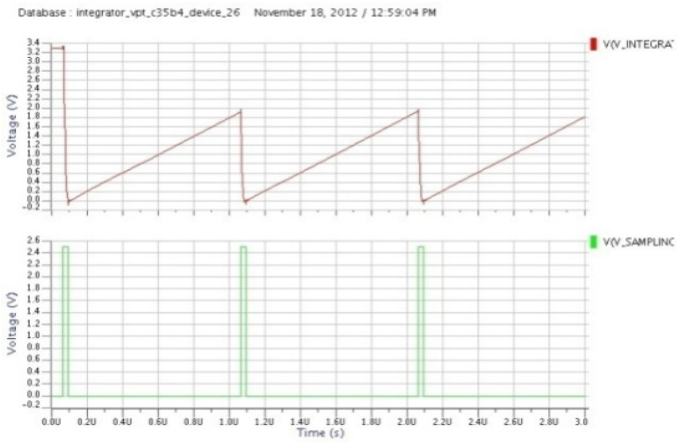

FIGURE X. RESULT OF INTERGRATOR AND S/H SIMULATION

The peak voltage of the integratoris 1.9 volts. There is a difference between voltage of the integrator with voltage of the reference.The difference of voltage of 2.0 to 1.9 = 0.1 volts. This difference is caused by the influence of the *Ron* on the transistors witch. Since the power supply of the integrator circuit is -3.3 volts until +3.3 volts, then the difference of voltage of 0.1 volts does not affect the circuit.

The integrator pulse is going down right when in contact with the pulse of S/H. The integrator period earned is 1 µs. This is in accordance with the input of clock input, e.i. 1 MHz. For application of ADC, the output of the integrator will be used as the input of the comparator and will be compared with the output of the S/H .

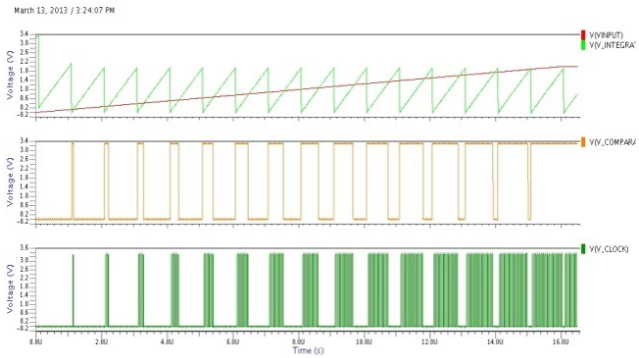

FIGURE XI. RESULT OF COMPARATOR SIMULATION

Based on Figure 2, right when the output of the integrator is in contact with the voltge of Vin, the output of the comparator will be low, and the data will be in the latch. The simulation result shows that when the voltage of the input is in contact with the output of the integrator, the comparator will close, and the enumeration of clock pulses equal to theperiod of t_c will happen.

Layout of analog unit presented in figure 12.

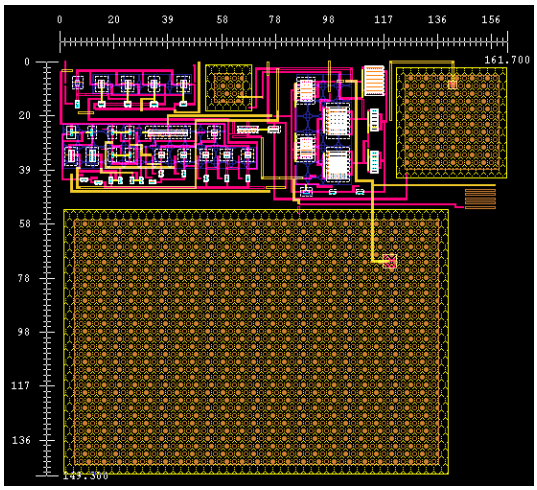

FIGURE XII. LAYOUT ANALOG UNIT

III. CONCLUSION

The result of the analog unit of ADC-SS designed remains optimal at the clock speed of 1 MHz . For the resolution of 8 bits, it earns V_{LSB}=7,8 mV. From the simulation result, it can be seen that the value of frequency of the integrator circuit is constant, so the quantization of ADC depends on the result of the enumeration of the input level to the amplitude of the integrator.

From some the simulation results, it needs a very precise calculations to generate ADC-SS design. Determination of value of the R and Cin the intergrator circuit must be precise, because the in accuracy of determinaton of the value ratio will result in a truncated integrator signal.

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