Synthesized Design Layout Base CMOS Technology 0.35μm

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***Abstract*—This paper deals with the manufacture of electronic design of digital systems with HDL programming language. HDL design synthesized using Leonardo Spectrum software, it means HDL design that has been designed to be compile on IC design technology, so it can be translated into the form of schematic and layout by using mentor graphics and ASIC Design Kit. To test the digital system using HDL programming language can be translated into schematic and layout, the design of the circuit to be tested several designs electronics starts with a simple circuit design, such as the design of boolean algebra expressions, an example for the application of control air temperature. Neither the complex circuit design, in terms of design consists of more than architecture or integrated circuit with a processor, such as use Gumnut Processor, So it can be create an electronic circuit system devices with high accuracy, and developing technologies based computer, such as smart management of energy technology system or technology and Secure Intelligent Transportation Systems.**

Keywords-component; mentor graphics; synthesized desaign digital; leonardo spectrum; ADK mentor graphics

I. INTRODUCTION

The development of modern digital systems is growing , include the design of embedded systems, now we can make digital system into design electronic circuit design with multiple targets technologies including from ASIC (Application-specific Integrated Circuit) technology and CMOS (Complementary Metal Oxide Semiconductor) with a size which until now has reached the technology μm (micro), because it can integrate the transistors in a single CHIP, then becoming known the development of semiconductor technology which is next called with VLSI (Very Large Scale Integration) [5] . The development of the technology of digital systems can be designed to create a design of an electronic circuit either as a series of simple design expressions boolean algebra, up to complex electronic circuit design, circuit complex in the means the design already in thousands of transistors are integrated with each other and have more than one function, or a multi-function [1].

To design of electronic circuits on a digital system in the field of design CHIP, at this time there is a design software which is also called the ECAD (Electronic Computer Aided Design) makes it easy for designers to design the circuit in the form of design and can be implemented in the form of process simulation [1]. Chip design software available today assorted one of which is the mentor graphics. Mentor graphics software has several supporting devices such as Leonardo Spectrum for synthesize of the digital system by using a programming language HDL (Hardware Description Language), and ADK (ASIC Design KIT) to translate from HDL into the circuit in the form of schematic and layout IC. So that the author can use simulate digital electronic circuits and can translate into form of IC.

In this paper discusses some of the circuit design in the design of digital systems using HDL programming language and translated in the form of schematic and layout IC using mentor graphics software and technology TSMC035.

Results from this paper may be a IC layout by using the output of the circuit simulation. Research focused on the process of using Leonardo Spectrum synthesis of HDL, starting with a simple circuit such as a series of boolean algebra expressions, up to complex circuits such as by using prcessor design, to be designed in the form of schematic and layout. With the aim to implement a series of quickly and appropriately to be synthesized in the form of IC layout.

II. SYNTHESIS DESIGN DIGITAL

A. *Preparation of Design and Constraint*

The first phase to design the path or is preparatory electronic circuits designed or required by the system. Preparations are in-fill purpose is to determine the (input) and output as well as the process of the circuit that you want to design. As one example, if we want to design a logic circuit two gate input, then the preparation must do design is to define two input variables , with a variable output, logic circuit and the arithmetic to multiplication calculations. After the preparatory stage design has been done, the next step is to use constraint as the determination of the assignment of each variable in the design of the design, and determine the output of the simulation of the design have designed, such as in determining the time of analysis (timing analysis) or rate setting signal (clock signal) [2].

B. *Design Process*

The next stage is the process of design, in this phase of the design that has been designed to be in the process of using the hardware programming language HDL. The process used as a predetermined design in programming languages, such as creating a variable to input and output, making the architecture

of the design that has been in design, and create constraint [2]. In this paper, used VHDL programming language .

C. Design Verification Test

In the test phase verification of design, a design that has been designed in a test in the form of signals with design objectives have been designed in accordance with the draft or not appropriate. The signal under test is entered, and the output signal, if the signal has not been tested in accordance with a design that is designed, stage is to do with the design process back [1]. Design verification test can be used with software ModelSim.

D. Synthesis

Synthesis on a design, a process for changing the original design file that is written in the programming language HDL into a new file that has been implemented by some of the technology and the rules. Technology and the rules of standard cell that contains a set of basic logic circuits which have been arranged by the library of technology, as a translator of a beam design to allow display circuits into a circuit schematic according to the standards of each technology [3]. Synthesis process in this study using Leonardo Spectrum 2014, with technology which available from Mentor ADK3,1 graphic. AMI technology and TSMC. In this study, using a synthesis process TSMC035 technology.

E. Verification Test After Synthesis

At this point of design that has been synthesized tested back form the signals, with the aim to verify output design before synthesis and design after synthesis have equally good results, thereby reducing the design error that has been designed from scratch [1].

F. Implementation In Physical Form Design

In this point after the design has been verified, and in accordance with the results of the preliminary design, the design which has been shaped HDL files will be translated into the physical design form or schematic form to be implemented into an IC layout at a later stage [4]. In this point of implementation of the HDL file into a schematic needed ADK from mentor graphic to translate into architectural schematic.

G. Phase of Building Design Layout

In this point, a build automatic layout design use ADK devices in mentor graphic. During the process of building a layout design, also implemented the technology used along with the rules of the technology that has been determined to create a layout, so the layout is displayed according to the standard of technology already automatically [1], for an example use the technology for layout is TSMC035.

H. Test

In this point, tests and trials are the last point in the design methodology. At this point layout that has been formed to test whether there is an error in the structure of the layout, or whether the layout that has been formed in accordance with the schematic design or design early [1]. If there is no error, the layout design is ready for use / printed in the form of IC.

III. Synthesis Design Layout Method

Synthesis design layout method used a systematic step to test a design, the method show in figure 1

FIGURE I. SYNTHESIS DESIGN LAYOUT METHOD

In figure 1, synthesis design layout method have done in 3 steps (white box). First the initial design (Desain VHDL), describe a design through a hardware programming language use VHDL. Second steps is making a netlist using Leonardo spectrum, Leonardo spectrum can synthesis the program design, so we can testing the design have mistake or not, if it no mistake, the design will be a netlist. Next steps is design constraint, function setting of each variables used, and to test the design in the form of signals. After process constraints, the next design is optimization (optimize) with standard cell technology used for further processing translate into schematic and layout [3].

IV. Result

After method of research have been succesed, Results will be tested is an electronic circuit designed, starting with the basic design of such a boolean algebra, up to the level of complex designs such as by using the Gumnut Processor, for example Air Temperature Circuit design and Alarm Digital Clock design..

A. Air Temperature Circuit

Air Temperature Circuit is basic electronic design who use a Boolean algebra, inspirated from [Peter Ashenden, 2006] book *Digital Design An Embedded Systems Approach Using VHDL. Morgan Kaufmann.* This circuit have logic design to create a simple control system, for example for air temperature control. Air temperature circuit can control air temperature with some conditions, for example if temperature low (*temp_rendah*) or hot condition (*panas_manual*) so the air temperature status is hot (*panas_on_temp)* and if temperature hight (*temp_tinggi*) or cold condition (*dingin_manual*) so the air temperature status is cold (*dingin_on_temp).* The circuit design and design after synthesis show below,

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity temperature_udara is
port  (
   temp_rendah, temp_tinggi, otomatis_temp :in std_logic;
   panas_manual, dingin_manual, angin_manual : in std_logic;
   panas_on, dingin_on, angin_on :out std_logic );
end temperature_udara;
architecture Behavioral of temperature_udara is
signal panas_on_temp, dingin_on_temp : std_logic;

begin
panas_on_temp <= (temp_rendah and otomatis_temp) or panas_manual;
dingin_on_temp <= (temp_tinggi and otomatis_temp) or dingin_manual;
angin_on <= panas_on_temp or dingin_on_temp or angin_manual;
panas_on <= panas_on_temp;
dingin_on <= dingin_on_temp;
        end Behavioral;
```

1) *Air temperature circuit*

```
module temperature_udara ( temp_rendah, temp_tinggi, otomatis_temp,
panas_manual,   dingin_manual, angin_manual, panas_on, dingin_on,
angin_on ) ;
   input temp_rendah ;
   input temp_tinggi ;
   input otomatis_temp ;
   input panas_manual ;
   input dingin_manual ;
   input angin_manual ;
   output panas_on ;
   output dingin_on ;
   output angin_on ;
   or03 ix11 (.Y (angin_on), .A0 (panas_on), .A1 (angin_manual), .A2
(dingin_on
       )) ;
   ao21 ix7 (.Y (panas_on), .A0 (otomatis_temp), .A1 (temp_rendah), .B0 (
       panas_manual)) ;
   ao21 ix3 (.Y (dingin_on), .A0 (temp_tinggi), .A1 (otomatis_temp), .B0 (
       dingin_manual)) ;
endmodule
```

2) *Air temperature circuit VHDL after synthesis*

After design have been synthesis, next step is simulation design show in figure 2.

FIGURE II. SIMULATION AIR TEMPERATURE CIRCUIT

If the simulation have same into desired design, next step the design will translate into schematic and layout who show in figure 3 and 4.

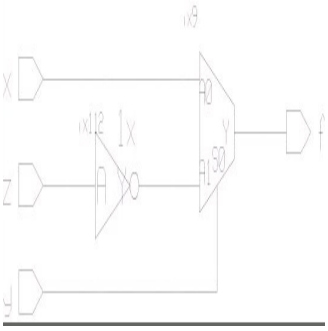

FIGURE III. SCHEMATIC AIR TEMPERATURE CIRCUIT

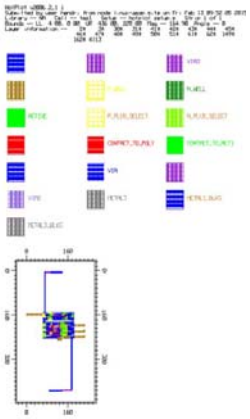

FIGURE IV. LAYOUT DESIGN AIR TEMPERATURE CIRCUIT

B. *Alarm Digital Clock Using Gumnut Processor*

Alarm Digital Clock using Gumnut Processor, is one of complex design inspirated from [Peter Ashenden, 2006] book *Digital Design An Embedded Systems Approach Using VHDL. Morgan Kaufmann*. The complex means structure desain more than architecture or integrated circuit with a processor. The structure must have alarm design, digital clock design, and gumnut processor design. All design must be combined and formed into one design, so it can have translated into schematic and layout. The design Alarm Digital Clock using Gumnut Processor with VHDL show in figure 7, and figure 8 show the design after synthesis.

```
…….
digit_reg : process (clk)
  begin
    if rising_edge(clk) then
      if reset = '1' then
        digit <= "1111";
      elsif port_cyc_o = '1' and port_stb_o = '1'
           and port_we_o = '1' and port_adr_o(0) = '1' then
        digit <= not port_dat_o(3 downto 0);
      end if;
    end if;
  end process digit_reg;

  seg_reg : process (clk)
  begin
    if rising_edge(clk) then
      if reset = '1' then
        seg <= "11111111";
      elsif port_cyc_o = '1' and port_stb_o = '1'
           and port_we_o = '1' and port_adr_o(1) = '1' then
        seg <= not port_dat_o;
      end if;
    end if;
  end process seg_reg;
……..
```

3) *Alarm digital clock VHDL*

```
gumnut_with_mem_false core (.clk_i (clk), .rst_i (reset), .port_cyc_o (
                port_cyc_o), .port_stb_o (port_stb_o), .port_we_o (
                port_we_o), .port_ack_i (port_ack_i), .port_adr_o ({
                \$dummy [0],\$dummy [1],\$dummy [2],\$dummy [3],
                port_adr_o_3,port_adr_o_2,port_adr_o_1,port_adr_o_0})
                , .port_dat_o ({port_dat_o_7,port_dat_o_6,port_dat_o_5
                ,port_dat_o_4,port_dat_o_3,port_dat_o_2,port_dat_o_1,
                port_dat_o_0}), .port_dat_i ({port_dat_i_7,
```

```
                port_dat_i_6,port_dat_i_5,port_dat_i_4,port_dat_i_3,
                port_dat_i_2,port_dat_i_1,port_dat_i_0}), .int_req (
                int_req), .int_ack (int_ack)) ;
  fake_vcc ix1156 (.Y (port_ack_i)) ;
  fake_gnd ix1154 (.Y (reset)) ;
  dff reg_int_req (.Q (int_req), .QB (\$dummy [4]), .D (nx1386), .CLK (clk)) ;
  mux21_ni ix1387 (.Y (nx1386), .A0 (nx1594), .A1 (int_req), .S0 (nx1596)) ;
  inv01 ix1595 (.Y (nx1594), .A (int_ack)) ;
  aoi21 ix1597 (.Y (nx1596), .A0 (nx1887), .A1 (nx294), .B0 (int_ack)) ;
  nor03_2x ix551 (.Y (nx1213), .A0 (nx1214), .A1 (count_7), .A2 (nx1883)) ;
  nand02 ix515 (.Y (nx1214), .A0 (nx1600), .A1 (nx1715)) ;
  nand02 ix455 (.Y (nx1216), .A0 (nx1603), .A1 (nx1696)) ;
  oai32 ix1237 (.Y (nx1236), .A0 (nx1607), .A1 (nx1879), .A2
(clk_1MHz), .B0 (
      nx1650), .B1 (nx1893)) ;
```

4) Alarm clock digital VHDL after synthesis

After Synthesis,next step is simulation design show in figure 5

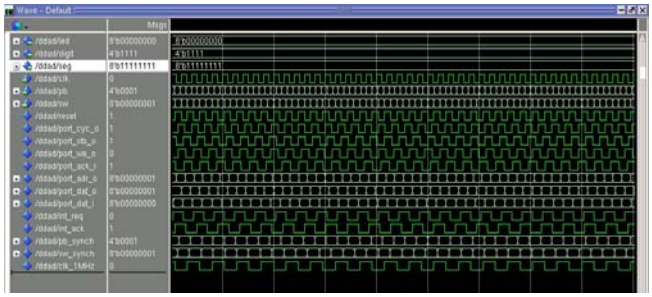

FIGURE V. SIMULATION ALARM DIGITAL CLOCK

After simulation, design can translate into schematic and layout design.

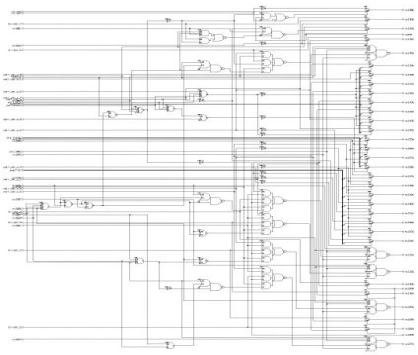

FIGURE VI. SCHEMATIC ALARM DIGITAL CLOCK

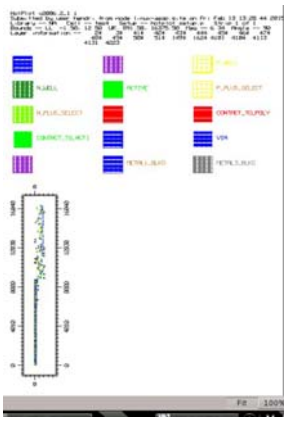

FIGURE VII. LAYOUT ALARM DIGITAL CLOCK

V. CONCLUSION

1. The digital system is able to design electronic circuit design from circuit stage such basic boolean algebra expressions, to complex designs such as the design stage of the circuit which is controlled by the processor, with minimum errors.

2. Synthesis desaign digital, afford to make some of the concepts of electronic circuits, and can translate into form of schematic and Layout IC, which was ready to be made or fabricated.

3. Synthesis of digital design has a new breakthrough for researchers who are interested ASIC design implementation to create electronic circuits and developing technologies based computer, such as smart management of energy technology system or technology and Secure Intelligent Transportation Systems.

REFERENCES

[1] [Chen[Peter Ashenden, 2006] Peter Ashenden, J. (2006). Digital Design An Embedded Systems Approach Using VHDL. Morgan Kaufmann

[2] [Crop, J, 2011] Crop, J. (2011). Design Automation Methodology For Improving the Variability of Synthesized Digital Circuit Operating in the sub/Near- Threshold Regime. /jurnal/IEEE Xplore Abstract (Abstract) - Design automation methodhology for improving the variability of synthesized digital circuits operatin.htm

[3] [Moustafa A. Sayed and Ehab Y. Abdel, 2009] Moustafa A. Sayed and Ehab Y. Abdel. (2009). Interconnect Synthesis In High Speed Digital VLSI Routing. Int. J. Open Problems Compt.Math.,Vol.2, No.3,September 2009

[4] [P.Pradeepa, etc.all, 2013] P.Pradeepa, etc.all (2013). Design And Implementation Of Vending Machine Using Verilog HDL. IJAET/Vol.IV/Issuee 1/Jan-March.,2013/41-53

[5] [David Harris And Neil H.E. Weste, 2005] David Harris And Neil H.E. Weste. (2005). CMOS VLSI Design. Pearson