# Design Analog Layout Using Schematic-Driven EDA Tools 

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#### Abstract

The method of Integrated Circuit (IC) Design using Electronic Design Automation (EDA) tools consists of (i) Full Custom IC Design and (ii)Automated IC Design. Schematicdriven layout on EDA tools has provided to facilitate designer madelayout design before fabrication, the core is to make it easier,faster, and short time consuming. Therefore in this paper will explain the process of make analog layout to redesign for multiplier circuit which is part of the cell of Analog neural network by using SDL. This circuit is designed using SDL with semi-Automated design method and $0,35 \mu \mathrm{~m}$ CMOS technology (Abstract)


Keywords-schematic driven layout; analog layout; CMOS design; multiplier

## I. Introduction

IC design consists of three parts: analog design, digital design and analog-mixed signal. In general, there are 2 of the IC design analog and digital design and there is a difference between them. digital design using standard cells or gates arrays with semicustom designs dan analog design using fullcustom design or manually design [3]. And the other hand, digital design using using modern well-developed cell-based tools for synthesis, mapping, and physical design. Then analog design normally has to be designed manually due to design complexity, fallibility, and low productivity because the design which occupies only a small fraction of the total chip area [4].

Matching (schematic and layout) is main concern when using an analog design because how well two identical transistors' characteristics match electrically which is is often the limitation in the quality of a design [7], but this not our focus. So an analog design could match well between schematic and layout, it can use the Schematic-Driven Layout (SDL) of EDA tools as a tool. This paper focus to make redesign layout of the circuit multiplier as case study that is part of a circuit analog neural networks which become current research [1][2]. Problems in making the layout redesign for this circuit is how to redisgn the layout easily, simple, quickly, and reduce or optimize layout area (size) then before [2] without having to do a full custum design. Therefore the design of this multiplier circuit using semi-Automated designs that use technology $0.35 \mu \mathrm{~m}$ from Austria Microsystems (AMS) with analog library of analog-mixed signal (Hit-kit) and Mentor Graphics Higher Education Program (HEP) Software as EDA tool.

This paper consists of 4 section, which section I will discuss the topic introduction, then the second section will
discuss study of literature, Design Flow Section III, section IV will describe the conclusion of this paper.

## II. Literature Study

## A. Multiplier Analog Neural Network

The Circuit neural network unit cell consists of (i)multipliers, (ii)OP-AMP, and (iii)sigmoid [1]. Multiplier circuit is used to do the calculations between input and weight given. Then the result of the multiplier circuit as a current. This result needs to be changed into voltage to ease calculation process. After the process then continued to Operational Amplifier (OP-AMP) for changed current into voltage. After the output of the OP-Amp obtained then the next process is to provide input (OP-Amp Output) to sigmoid. This sigmoid function to generate activation functions for neurons. At the beginning of the design of neural networks that are based on a single architecture perceptron and Figure 1 as we proposed to redsign [1][2].


FIGURE I. UNIT CELL ARTIFICIAL NEURAL NETWORK WITH SDL [1]

## B. Analog Layout

CMOS circuits is a set of PMOS and NMOS transistors interconnected. To implement the CMOS circuit into physically (IC) then in need of a layout. Typical of analog layout is the calculation of the aspect ratio $(\mathrm{W} / \mathrm{L})[6]$ of the transistor shown in the figure 2.


FIGURE II. LAYOUT OF PMOS [6]

The main thing of concern in designing the layout of transistors following [6]:

- parasitic resistances at source and drain must be kept as low as possible.
- parasitic capacitances should be minimized.
- matching between paired elements is very important


## C. IC Design EDA Tool

- Custom Layout vs Automated Layout

Full custom, or handcrafted IC design, is process of creating an ic by manually creating and editing each polygon and generally gives the most compact design [8]. Automated layout is the process of creating an IC by placing cells into a layout performing automatic routing between the cells to generate an IC layout from schematics or from netlist information [8]. Mentor Graphics provides CAD tools realizing front-end design flow of custom IC [5].

## - Schematic Driven Layout

Schematic Driven layout is a design methodology that allows a designer (Design Enggineers) to make the correct or exactly match layout construction or design method which uses schematic followed by layout which components are instantiated from schematic in a correct by construction [3]. The concept of Schematic driven layout is where the software of electronic design automation (EDA) connecting between schematic and layout. Section which is connected to the SDL process is database of the schematic and layout.

By using SDL is expected to (i)make it easier to produce a layout according to the schematic, (ii)Assist in the placement and route of Cells or device on the layout. (iii)for interactive communication between the schematic and layout in terms of checking the layout. (iv)Reducing or save the time of making the layout phase. On the other hand using SDL can achieve result that very close to full custom manual layout[3].

Sources that can be used to create layouts using SDL is Viewpoint. Viewpoint is a component of the design as a place to store the configuration of the schematic [9]. Viewpoint can be generated using the HIT-KIT from AMS. Viewpoint level consists of three levels are device, Cell and appar. viewpoint is divided into 4 parts [9]:

1) $v p t_{-}<$tech>_cell used for: level verilog netlist creation for Modelsim simulation.
2) vpt_<tech>_apar used for :Place dan route ( $\mathrm{P} \& \mathrm{R}$ ) with IC-Station, SDL flow on Cell/Block level with IC-Station.
3) vpt_<tech>_device used for : Device primitive netlist creation for Eldo and ADMS simulation (for Mixed signal simulation the 'view' property is used to prevent the EldoNet netlister from going down if the view below the symbol is not 'schematic'), SDL flow with IC-Station

## III. DESIGN FLOW

There are 9 phases of design flow, For 4 steps first is logic level and 5 steps second is physical level [5]. Circuit schematic of a multiplier previously been made and through
the simulation phase [1][2]. Making the multiplier circuit schematic design entry using the software "Design ArchitectIC" which is part of ICFLow. The process of making the schematic using the library (library) technology with the name "HIT-KIT 3.70". This reason the method SDL using semiautomated design, which is CMOS components used NMOS4 and PMOS4 has been defined in library technology. then continued with the placement (Device and port) and routing process.

This Circuit consists of 17 components MOS (7PMOS + 10 NMOS ), there is no resistor and capacitor. There are 7 Port (6 Port Enter and 1 Port Output). Port Input consists of VDD (Source Voltage), GND (Ground), VSS, VBias X, and Y. Port Output namely Z.


FIGURE III. MULTIPLIER MODIFIED CIRCUIT
The steps in making the layout using SDL are following 3 :

1) Creating Design Viewpoint.
2) Creating Cell.
3) Placement Devices.
4) Placement Ports.
5) Routing.

## A. Creating Viewpoint

Viewpoint making process using the Design Architech-IC. Viewpoint is made by utilizing the facilities provided in the HIT-KIT with the name austriamicrosystem DVE (Viewpoint Design Environment). Viewpoint level used is apar. Viewpoint apar Was chosen because it can to use for the
layout with the P \& R (Place and Route). The process of making viewpoint is stored in a file with the name "vpt C35B4 apar". Fig 4 shown as Viewpoint Process and Fig 5 shown as Viewpoint File Configuration


FIGURE IV. VIEWPOINT PROCESS


## B. Creating Cell

Creating multiplier cell performed using the Invoking ICStation. This process involves the design viewpoint that has been made on the schematic. The design viewpoint connected with a layout that will be created. Fig 6 shown as the Creating multiplier cell process.


FIGURE VI. CREATING MULTIPLIER CELL PROCESS

## C. Placement

We arrange (PMOS and NMOS) by grouping based on the type of device. PMOS on top and nmos on bottom shown on fig 7.


FIGURE VII. PLACEMENT PLAN

## 1) Placement Device

At this phase the placement of devices made using the facilities Automated Design Layout (Layout DLA). The first phase is the placement of devices. Placement of devices performed by using the "insert". In the placement process does not use "autoinsert". Placement is done manually, because if used autoinsert then the resulting layout does not fulfill design rules. Fig 8 shown as Result Placement Devices.


FIGURE VIII. PLACEMENT PLAN

## 2) Placement Ports

Then the Ports placement performed using the "Port" function. This placement serves to put the ports in accordance with the schematic drawing and also simplify the placement of ports. There are 7 ports, VDD, VSS, Vbias, X, Y, Z, Ground. Fig 9 shown as Placement VDD Port.


FIGURE IX. RESULT PLACEMENT DEVICES

## D. Routing

After the placement phase is completed then proceed with the routing phase. This phase is the process of connecting paths between device to device and device to ports. Connecting paths can be performed using two methods, namely "aroute" and "iroute". "Aroute" work automatically connects the path but not all paths can be connected. "Iroute" can connect paths manually in accordance with the path that we wanted. Fig 10 show Yellow Lines as the guidelines. This line is formed when beginning the process of SDL. With this line the path connection process becomes easy.


FIGURE X. RESULT PLACEMENT DEVICES

## E. Result

After the previous phases, placement devices, placement ports and routing device to device, routing device to port then the results obtained layout as shown in fig 11.


FIGURE XI. LAYOUT RESULT

## IV. Conclusion

By using SDL with semi-automated design can easily create layouts and shorten the time. Although this design made from semi-automated design was able to setting the layout size by adjusting the distance between the devices and the paths between devices. This settings made easy with the guide lines are yellow on the routing process. Then from the SDL phases can be continued to verification layout. But in verification layout has problem, because process Design Rule Check (DRC) and Layout Versus Schematic (LVS) needed more time consumed. therefore, future work the problem can be the next discussion.

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