Cascaded Sigma-Delta modulator with dual quantization architecture and an inter-stage feedback path

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Abstract. The conventional Sigma-Delta modulators have several drawbacks: e.g. the major problem with dual quantization architecture is that it can only be applied in a single loop topology, which causes the dynamic range (DR) problem; The inter-stage feedback topology only cancels nonlinear errors by introducing multi-bit DAC in its final stage. However, the rest of the stages still contain DAC nonlinearity errors without any noise shaping, which still degrade overall system performance. We propose a new structure, specifically a third-order (1-2) cascaded Sigma-Delta modulator with two 1-bit quantizers and an inter-stage feedback path. The main advantage is its 6dB reduction of total output noise power as compared with a conventional second-order Sigma-Delta modulator. We derive the output expression of various Sigma-Delta modulators in closed form. The advantage of the proposed modulator is confirmed by a system level simulation program.

I. INTRODUCTION

The Sigma-Delta modulator with a multi-bit internal quantizer offers many advantages, such as, first, it reduces the quantization error in every bit. Therefore, a better SNDR can be attained, and more stability can be achieved due to limiting the variation of the effective gain of the quantizer. Second, it allows lower power dissipation[1], because the requirement of linearity on the input stage is also constrained. However, unfortunately, any nonlinear error caused by the multi-bit DAC will limit the benefit of noise shaping and produce nonlinear signal distortion into the overall ADC response.

To overcome such a problem, many improved versions of the Sigma-Delta modulator are proposed, such as, ones that use dual quantization architecture[2] and inter-stage feedback paths[3]. The main advantage of the former is that it uses only a single-bit feedback and hence effectively avoids the matching problem which is inherent in a multi-bit feedback DAC. However, it can only be applied in a single loop topology, which causes the Dynamic range (DR) problem. The main advantage of the latter is that it totally cancels the DAC nonlinearity errors of the final stage due to extra feedback paths in each internal stage. However, the remaining stages also contain DAC nonlinearity errors, which still degrade overall system performance. We propose a new cascaded multi-bit Sigma-Delta modulator, which cancels nonlinearity errors induced by DAC in each stage without scarifying DR performance. We will derive the output expression of various Sigma-Delta modulators in closed form, including the conventional ones. Simulation results will validate the superiority of the proposed modulator.

II. PROPOSED CASCADED MULTI-BIT SIGMA-DELTA MODULATOR

If we can scale down the noise by a constant factor while keeping the signal unscaled, then the total noise power at the output, as well as the low-frequency noise power, will be further decreased. These in turn will lead to a higher signal-to-noise ratio and a relaxed requirement on the following digital filter. However, it has been shown that there is no way to scale down the quantization noise by a constant factor (while keeping the signal unscaled) in a Sigma-Delta modulator with one quantizer due to the delay requirement of the noise shaping loop[4].

The proposed modulator contains two stages shown in Fig. 1. The first stage adopts a multi-bit quantizer, while the other stages use multi-bit quantizers to achieve higher SNDR (Signal to Noise and Distortion Ratio). The output of DAC in the second stage directly feedbacks to the first stage, and nonlinearity errors of DAC can be totally suppressed by two digital cancellation logics: $H_1(z)$ and $H_2(z)$. In the first stage, it can be derived

$$\left(X(z)-Y_1(z)-E_{d1}(z)\right)\frac{z^{-1}}{1-z^{-1}}-E_{d2}(z)-Y_2(z)+E_1(z)=Y_1(z) \tag{1}$$

$$\begin{aligned} Y_1(z)\left(1-z^{-1}\right)=\left(X(z)-Y_1(z)-E_{d1}(z)\right)z^{-1}-E_{d2}(z)\left(1-z^{-1}\right) \\ -Y_2(z)\left(1-z^{-1}\right)+E_1(z)\left(1-z^{-1}\right) \end{aligned} \tag{2}$$

From Eq.(2), the first stage output of modulator can be attain

$$\begin{aligned} Y_1(z)=X(z)z^{-1}-E_{d1}(z)z^{-1}-E_{d2}(z)\left(1-z^{-1}\right) \\ -Y_2(z)\left(1-z^{-1}\right)+E_1(z)\left(1-z^{-1}\right) \end{aligned} \tag{3}$$

where $X(z)$ is input signal, $E_1(z)$, $E_{d1}(z)$ and $E_{d2}(z)$ are quantization noise in the first stage, and $E_{d1}(z)$, $E_{d2}(z)$ are nonlinearity error for multi-bit DAC from the first and second stage, respectively. In the second stage, it can be derived

$$\begin{aligned} 2Y_2(z)=\left(Y_2^{'}(z)-Y_2(z)-E_{d2}(z)\right)2\frac{z^{-1}}{1-z^{-1}} \\ +E_3(z)+2Y_2^{'}(z)+E_2(z) \end{aligned} \tag{4}$$

$$2Y_2=-2z^{-1}E_{d2}+\left(E_2+E_3\right)\left(1-z^{-1}\right)+2Y_2^{'} \tag{5}$$

$$Y_2^{'}=\left(E_1+E_{d1}-E_{d2}-Y_2\right)\frac{z^{-1}}{1-z^{-1}} \tag{6}$$

According to Eq.(4), (5)and (6), the second stage output of modulator can be attained

$$Y_2=z^{-1}\left(E_1+E_{d1}-E_{d2}\left(2-z^{-1}\right)\right)+\frac{E_2+E_3}{2}\left(1-z^{-1}\right)^2 \tag{7}$$

To effectively suppress the nonlinearity error and quantization noise, we propose to utilize jointly dual-quantization architecture and an internal stage feedback path. Therefore the final output is given by

$$Y(z)=Y_1(z)H_1(z)+Y_2(z)H_2(z) \tag{8}$$

where the digital cancellation logics can be represented as,

$$H_1(z)=z^{-1},\quad H_2(z)=(1-z^{-1})^2 \tag{9}$$

The final output can be reduced to

$$\begin{aligned} Y(z)=X(z)z^{-2}-E_{d1}(z)z^{-1}+E_{d2}(z)z^{-1}\left(1-z^{-1}\right)^2 \\ -\frac{E_2(z)+E_3(z)}{2}\left(1-z^{-1}\right)^3 \end{aligned} \tag{10}$$

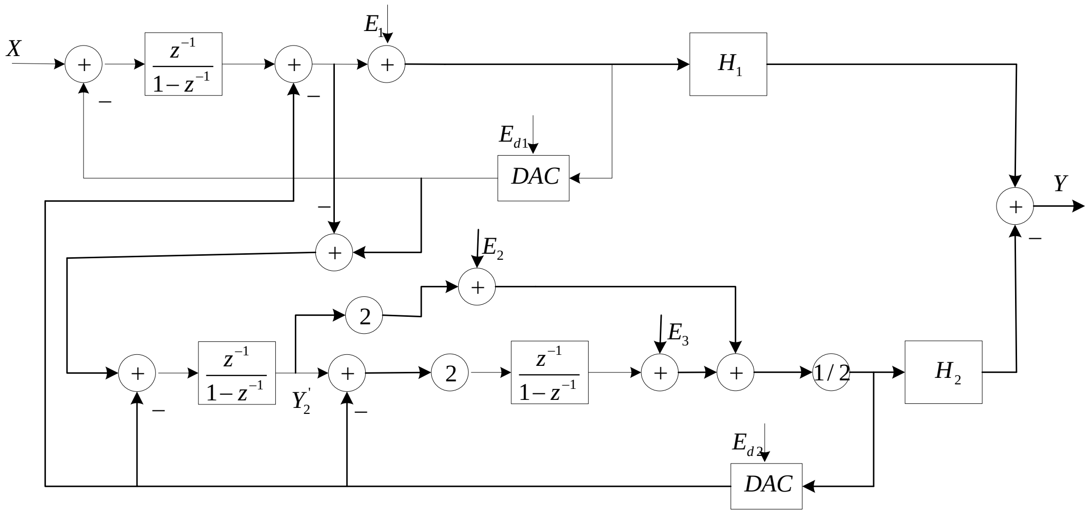

Fig.1 The proposed Cascaded Sigma-Delta modulator

III. SIMULATION RESULTS

We assume a 4-bit quantizer is adopted in all the cascaded Sigma-Delta modulators mentioned above. The other model parameters are summarized in Table I. Here we focus only on the effect of DAC nonlinearity errors, and other modulator non-idealities are omitted, such as sampling jitter and KT/C noise [5]. The power spectrum density (PSD) of various modulators is represented in Fig. 2. An SNDR of 70.7dB and 51.8dB can be achieved by the proposed modulators and the one described in [6], respectively. From Fig. 2, we can see that the proposed modulator has less SNDR losses.

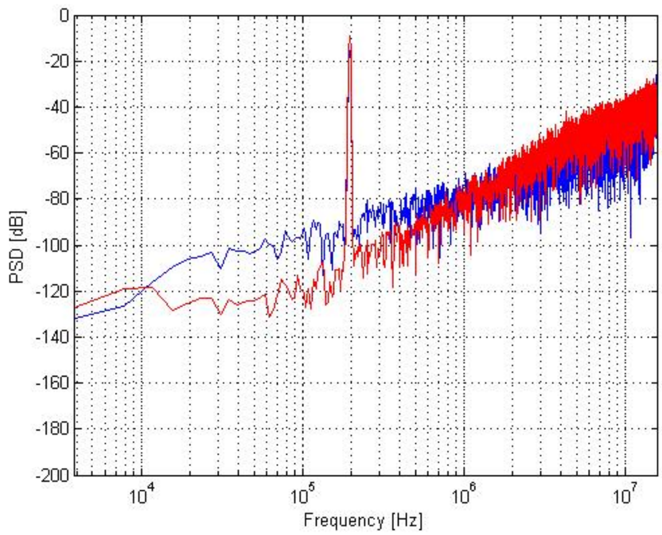

Fig.2 PSD (power spectrum density) comparison

Fig.3 shows a comparison of dynamic ranges (DR) in which the level of input signal changes from -20dB to 0dB. Fig. 3 shows that the proposed modulator still has a superior DR performance as compared with the conventional ones. The DR performance of the proposed modulator does not deteriorate until the level of input signal reaches -1dB, whereas such a case also occurs in the conventional ones even earlier.

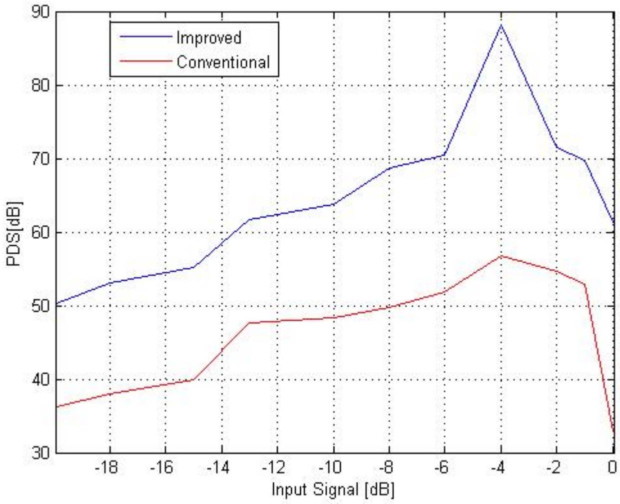

Fig.3 Dynamic range comparison

TABLE IPARAMETERS FOR SIMULATION

Parameters	Values
Input signal frequency	0.2MHz
Signal bandwidth	0.5MHz
OSR	16
Oversampling frequency	32MHz
Quantizer bits	4bit
Total capacitance for DAC	2pF
Capacitor standard deviation	0.0245

IV. CONCLUSION

In this letter we propose a new cascaded multi-bit Sigma-Delta modulator to resolve DAC non-linearity errors and derive the output expression of various Sigma-Delta modulators in closed forms. Simulation results show that the proposed modulator has a superior immunity against DAC nonlinearity errors as compared with conventional modulators.

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REFERENCES

[1] T. G. C. SCHREIER R, "Delta Sigma Data Converters," *IEEE Press*, 1997.

[2] J. Markus and G. C. Temes, "An efficient ΔΣ ADC architecture for low oversampling ratios," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, pp. 63-71, 2004.

[3] S. Amornwongpeeti, M. Ekpanyapong, and C. Punyasai, "A comparative analysis of behavioral simulation for third-order cascaded multi-bit Sigma-Delta modulator with interstage feedback paths," in *Electrical Engineering/Electronics Computer Telecommunications and Information Technology (ECTI-CON), 2010 International Conference on*, pp. 371-375.

[4] N. D. o. E. E. Tan, Linkoping Univ. Eriksson, S "Noise shaping with bilinear integrators " *Circuits and Systems*, pp. 1392 - 1395 vol.2, 1992., Proceedings of the 35th Midwest Symposium on.

[5] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto, and F. Maloberti, "Modeling sigma-delta modulator non-idealities in SIMULINK(R)," in *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, 1999, pp. 384-387 vol.2.

[6] L. Chun-Chen, C. Yung-Shan, and V. Balakrishnan, "On reduced-order filter design for uncertain cascaded 2-1 sigma-delta modulators," in *System Science and Engineering (ICSSE), 2011 International Conference on*, pp. 212-217.