Design and Realization of Pulse Compression Method of Radar System Based on FPGA

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Abstract. To solve the conflict between the radar range and distance resolution effectively, this paper design and realize a method of pulse compression of radar system. Firstly, the paper describes the working principle of pulse compression. Then a method of pulse compression simulation is designed based on chirp signal and frequency domain filtering design. And the softwares of Matlab and Modelsim are used to the simulation of this method .Finally, the design is downloaded to the chip of Field Programming Gate Array and realizes the pulse compression of chirp signal. The experimental results show that the method described in this article realizes the pulse compression of radar system and has certain feasibility and practicability.

Introduction

The use of linear frequency modulation (LFM) signal in radar system, can obtain high range resolution, and it can increase the range of radar. At the same time, it has good anti-jamming capability and low probability of intercept[1].

Range resolution for given radar can be significantly improved by using very short pulses. Unfortunately, utilizing short pulses decreases the average transmitted power, which can hinder the radar's normal modes of operation, particularly for multi-function and surveillance radars. Since the average transmitted power is directly linked to the receiver SNR, it is often desirable to increase the pulse width while simultaneously maintaining adequate range resolution. This can be made possible by using pulse compression techniques[2]. This paper is to study LFM signal pulse compression based on FPGA. The purpose is to find a method to realize LFM signal pulse compression by using FPGA.

Principle of Pulse Compression and Matlab Simulation

Processing the receipt signal, we need to set a matching filter to make broad pulse echo signal into narrow pulse for high range resolution[3]. For the deterministic signal, we can give the matching filter from the idea getting maximum output signal-to-noise ratio in receiver under the background of stationary Gaussian white noise[4].

$$\mathrm{H}(f) = \mathrm{k}\mathrm{S}^{*}(f)\exp\left(-j2\pi f t_0\right) \tag{1}$$

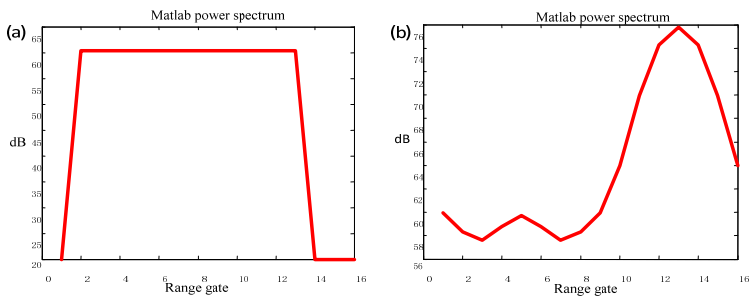
$\mathrm{H}(f)$ is the transmission characteristics of best receiving filter we are looking for. The pulse width ratio is called pulse compression coefficient D[5].

$$D = \mathrm{T}/\tau = TB \tag{2}$$

We can make pulse compression in time domain or frequency domain[5]. Time domain pulse compression processing is time-domain convolution between a Finite Impulse Response (FIR) filter and the echo sampling sequence[3,5], but the multiple correlation computation of FIR filter increases significantly when the time width of signal increases[5,6].

We choose frequency domain method to realize LFM signal pulse compression. Signal: $S(t) = rect\left(t/T\right) * \exp\left(j\pi kt^2\right)$, $t = -T/2 \sim T/2$, where, T is Time Width, 2 μs. K: LFM Signal Slope, B/T. B: LFM Signal Bandwidth, 2.5MHz. PRI: Pulse Repetition Interval, 23 μs. f_s: Sampling Frequency, 6MHZ. Target Number: One. Object Distance: 325 meters.

In real application, we do I/Q decomposition to the received radar echo signals, then do pulse compression. The method of dechirp technology in receiving echo need only a low sampling frequency, but range window limits deeply the range of measuring target[7]. And direct receipt can avoid this problem[7]. In this paper, using FFT + complex multiplication + IFFT method for pulse compression, you can also use CORDIC algorithm to realize pulse compression[8,9]. The results of 16 points pulse compression simulation are in Fig. 1.



(a) Before pulse compression (b) After pulse compression (D=5)

Fig. 1. Matlab simulation power spectrum of pulse compression

Implementation Approach of Pulse Compression on FPGA

Overall Scheme of Pulse Compression. Overall scheme of frequency domain pulse compression based on FPGA is shown in Fig. 2.

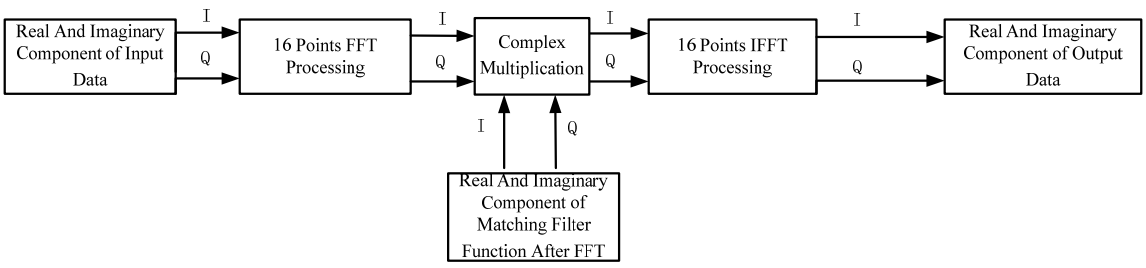


Fig. 2. Principle block diagram of overall scheme

Realization of FFT Module. FFT algorithm is basically divided into two categories: Decimation-In-Time FFT (DIT-FFT) and Decimation-In-Frequency FFT (DIF-FFT)[10]. This article take Decimation-In-Time FFT and radix-4 algorithm.

This paper adopts a cascade structure to implement the FFT processor[11]. According to different radix, cascade structure is divided into several levels, and each level use a butterfly computing unit. So that each level only complete the certain operation, and put the calculation results of the previous level into a ping-pong cache, next level read data from the cache in the form of assembly line. For radix-4, there is the number of $\log_4 N$ of butterfly computing units. Because the butterfly computing units between all levels works as assembly line, it has the acceleration effect for continuous multiple sequences of input. The cascade structure of FFT is shown in Fig. 3.

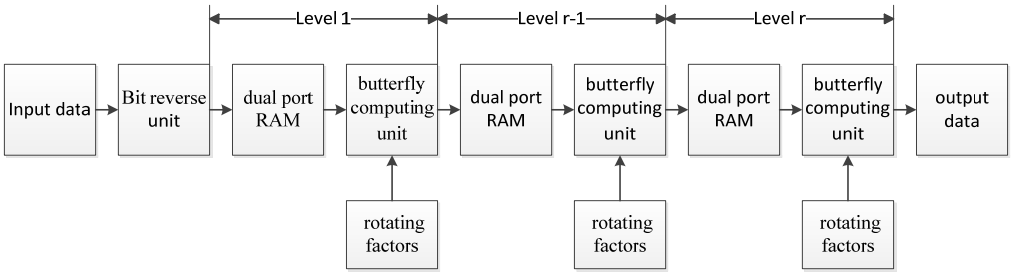


Fig. 3. Cascade structure of FFT module

Realization of IFFT Module. IFFT processing module and FFT processing module can share the same computing module, the theory is shown as follows, input data are X(k) and output data are x(n).

$$x(n) = IDFT[X(k)] = \frac{1}{N}\sum_{k=0}^{N-1} X(k) W_N^{-kn} \tag{3}$$

$$x^*(n) = \frac{1}{N}\sum_{k=0}^{N-1} X^*(k) W_N^{kn} = \frac{1}{N} DFT\left[X^*(k)\right] \tag{4}$$

$$x(n) = [x^*(n)]^* = \frac{1}{N}\{DFT[X^*(k)]\}^* \tag{5}$$

We can call FFT module to realize the fast computing of inverse discrete Fourier transform (IDFT), and realization method is:

a) Get $X^*(k)$, the conjugate of $X(k)$.
b) Call FFT module to compute the value of $DFT[X^*(k)]$.
c) Take the conjugate of the output data.

Realization of complex Multiplication Module. If we multiply $x_r + jx_i$ by $\cos\alpha - j\sin\alpha$, we can get real and imaginary component of the results:

$$y_r = x_r \cos\alpha + x_i \sin\alpha \tag{6}$$

$$y_i = x_i \cos\alpha - x_r \sin\alpha \tag{7}$$

It can be found that we need 4 real multiplying unit and 2 real adder in a complex number multiplication. Now, transform Eq. (6) and Eq. (7), we can obtain Eq. (8) and Eq. (9).

$$y_r = (x_r + x_i)\cos\alpha + x_r(\sin\alpha - \cos\alpha) \tag{8}$$

$$y_i = (x_r + x_i)\cos\alpha - x_r(\sin\alpha + \cos\alpha) \tag{9}$$

Thus it only needs 3 real multiplying unit and 5 real adder in a complex number multiplication. Through the transformation, reduce one real multiplying unit. Consumption of logical units of real adder is far less than real multiplying unit, so it can greatly reduce the consumption of resources.

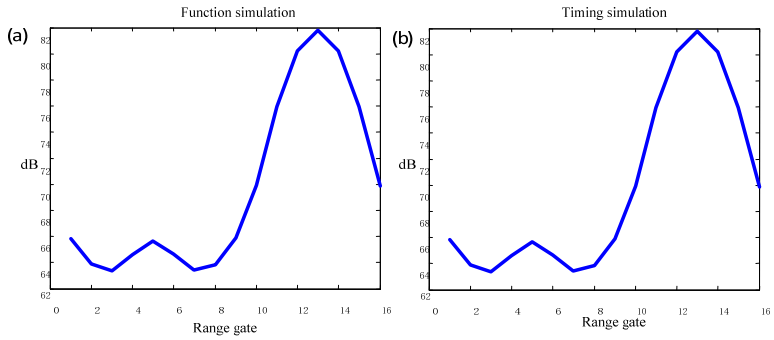
Modelsim Simulation of Implementation Approach. With the use of Modelsim, we do function simulation and timing simulation for general plan and the modules of pulse compression. We can deal with the results by Matlab, and verify the validity of pulse compression.

Results of simulation are shown in Fig. 4.

Result of Development Platform

The design of pulse compression method of radar system is realized on SmartSOPC development platform. The experiment result of 16 points FFT pulse compression on SmartSOPC development platform is shown in Fig. 5.

The results from FPGA experiment have some difference caused by hardware delay with simulation results of Matlab and Modelsim. But we can see that broad pulse become narrow pulse, and peak value appear in the right location where is the falling edge of the pulse before pulse compression, which correspond with results of Matlab and Modelsim simulation. In general, the results of experiment on SmartSOPC development platform reach the effect of pulse compression.



(a) Function simulation (b) Timing simulation(D=5)

Fig. 4. Power spectrum of Modelsim simulation

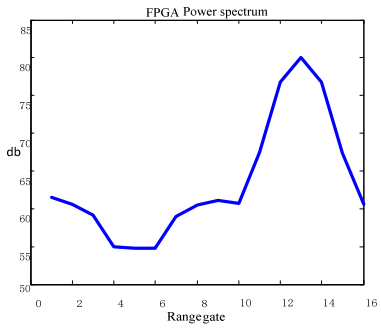


Fig. 5. Power spectrum based on FPGA(D=5)

Conclusions

This paper comes up with a pulse compression method of LFM signals and matching filter in frequency domain based on the summary of pulse compression. And use Matlab software to do theoretical simulation of pulse compression method. It is mainly described that implementation approach of pulse compression based on FPGA and Modelsim simulation for realization of pulse compression. Last, the LFM signal pulse compression method of radar system is realized on the SmartSOPC development platform. The advantage of FPGA is the high speed calculation and the flexibility of design. The experimental results show that the method described in this article has certain feasibility and practicability.

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