

## Real-Time Signal Acquisition System for Multi-Channel Bioelectrical sensing Application

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**Abstract.** This paper presented a high speed data acquisition system for real-time bioelectrical sensing application. The hardware of system mainly consists of data acquisition, distribution and storage section. Four dual-channel ADCs are applied in acquisition section. In distribution section, the original data stream will be distributed into four streams. Each data stream will be stored into one solid-state storage card which is composed of NAND flash array. Results of system evaluation show that system achieved good SNR (up to 70dB).

### Introduction

In computer science, real-time is the study of hardware and software systems that are subject to a "real-time constraint"—for example, operational deadlines from event to system response. Real-time system must handle the processing load within strict constraints on response time. In data acquisition application, real-time means that the acquisition system could acquire and store each input signal at system's sample rate without missing or error.

With the development of science and technology, the bandwidth of signal is increasing rapidly in bioelectrical measurement applications [1, 2]. That needs acquisition system has higher sample rate and faster storage speed for storing acquired signal in real-time. But due to the limit of physical structure, the storage speed of traditional mechanical hard drive cannot meet high speed acquisition requirement.

Solid-state storage technique is a method of data storage accomplished by using integrated circuit devices to store data rather than moving magnetic or optical media[3]. It delivers ultra-fast random data access, low power consumption, small size and high physical resilience (due to no moving parts). By using solid state storage technique in high speed data acquisition system, the total storage bandwidth could be improved significantly. That makes high-speed real-time data acquisition technique become feasible.

This paper discussed a design and implementation method of a high-speed real-time data acquisition system for bioelectrical sensing application.

### Hardware Design

The architecture of our system is shown in Fig.1. The system is mainly consists of 3 parts: acquisition section, distribution section and storage section. The acquisition section includes ADC and its external circuits (signal conditioning and clock circuits). The data distribution section is used for decreasing the speed of data bus by increasing bus width. The original parallel data from ADC will be distributed to four group serial data. The separated data streams will be transferred by serial transport protocol and stored into solid-state storage card which composed of NAND flash array. The stored data could be read back to computer memories by PCI-E bus. Finally, data will be merged into original one in computer and for further processing.

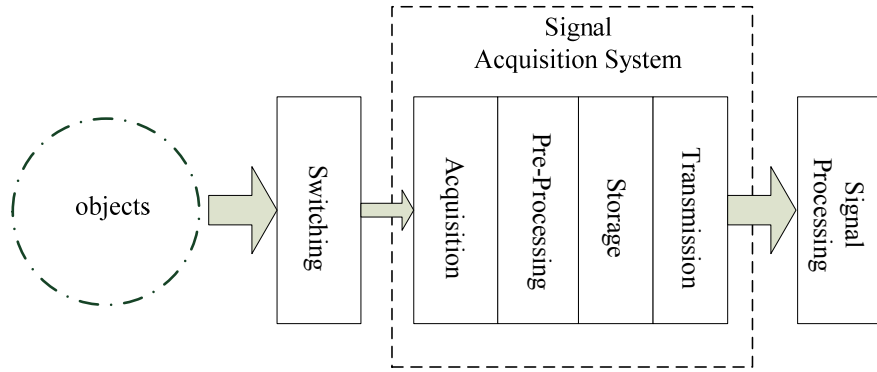


Figure 1. Hardware Architecture of Real-time Data Acquisition System.

### Acquisition Section

The acquisition section is mainly composed of signal conditioning circuit, analog-to-digital converter (ADC) and clock generator. The signal conditioning circuit includes 6 stages. The first stage is input impedance matching circuit, which is used for matching impedance between acquisition section and input signal source. The second stage is attenuation circuit, for attenuating the over-range input signal into buffer's input range. The third stage is buffer amplifier which provides impedance transformation from external circuit to internal circuit. Filter circuit is the 4th stage, which could remove unwanted frequency components in input signal. The 5th stage is gain adjusting circuit, which used to adjust the amplitude of signal to meet the input range of ADC. ADC matching circuit is the final stage, provides impedance matching between signal conditioning circuit and ADC device. The brief diagram of signal conditioning circuit is shown in Fig.2.

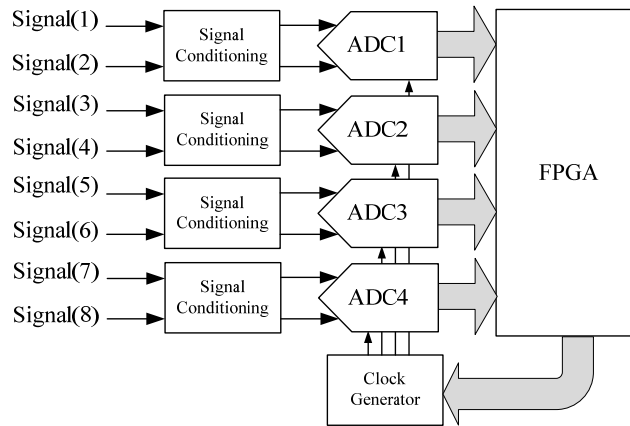


Figure 2. Diagram of Signal Conditioning Circuit.

In order to generate 4 way high speed clocks, we selected ADI's AD9517-4 as sampling clock generator for ADC operating[4]. It provides a multi-output clock distribution function with sub-picoseconds jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 1.45 GHz to 1.80 GHz. The AD9517-4 emphasizes low jitter and phase noise to maximize data converter performance, which is suitable for our data acquisition applications.

### Pre-Processing Section

Pre-Processing section consists of field programmable gate array (FPGA), clock generator, double data rate type three synchronous dynamic random access memory (DDR3 SDRAM) and small form-factor pluggable (SFP) modules.

We selected Xilinx's Virtex-6 serials FPGA as core of pre-processing section. In our application, type XC6VLX130T has been applied. With its 128000 logic cells and 20 GTX low-power transceivers, we can realize the high levels of performance and functionality into our system[5]. Every four GTX transceivers were combined as a group for serial transport which will be discussed below. SFP is used for converting electrical signals into optical signals, which could be transferred in optical fibers. For buffering the high speed data, we applied DDR3-1066 modules which can archive transfer rate up to 8533MB/s using both rising and falling edges of a 400–1066 MHz I/O clock.

## Storage Section

The core part of storage section is a solid-state storage card. It primarily consists of FPGA, DDR2-SDRAM and NAND flash array. The distributed data is sent to the FPGA via optical fiber. Then the FPGA write the data into NAND flash array. DDR2-SDRAM is used as data buffer to improve random write/read speed. To meet the acquisition speed requirement, we built the array with 72 NAND flash devices. The read back data will be converged at the second FPGA and send to computer memories by PCI Express bus.

## Transmission Section

In our application, Direct Memory Access (DMA) technique is applied in PCI-E transmission for improving bandwidth and reducing the resource-consuming of CPUs. DMA is a feature of modern computers and microprocessors that allows certain hardware subsystems within the computer to access system memory for reading and/or writing independently of the central processing unit.

The architecture of implemented PCI-E DMA transfer module is shown in Fig.3. It consists of three major parts: Xilinx PCI-E hard IP, DMA manager and application interface. Xilinx hard PCI-E IP could realize x8 PCI-E communication by using GTP transceivers of FPGA. It provides the full functionality of the transaction layer, the data link layer, the physical layer, and the configuration space as PCI-E specification. The DMA manager module includes master module, slave module, configuration monitoring module and interrupts module. Master module is responsible for sending transfer requests issued by DMA channels to the transmit interface and receiving completions from the receive interface and forwarding them to the appropriate channel. The slave module handles target-mode read and write access to a memory-mapped on-chip SRAM and registers[5]. The configuration monitoring module is used to monitor the configuration message and the interrupts module handles interrupts message from application logic. The application interface comprises FIFO and data/address control logic, which is convenient for connection with user logic.

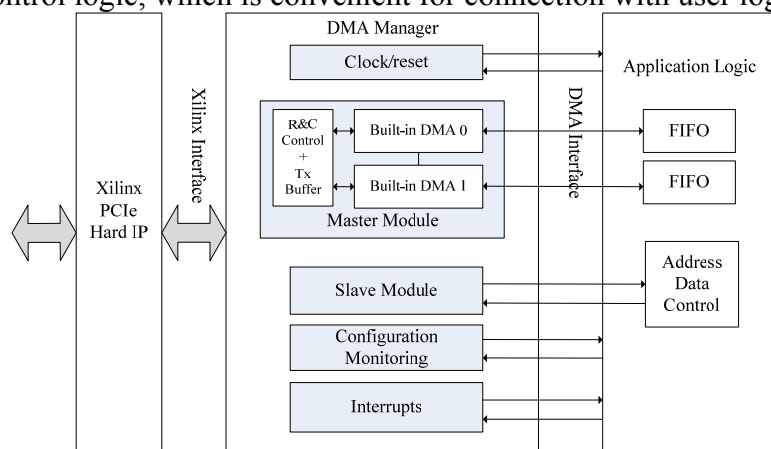


Figure 3. Architecture of PCI-E DMA Transfer Module

## System Evaluation

Signal-to-Noise Ratio (SNR) is a critical parameter of acquisition system. In order to test the SNR performance, we acquired the standard sine-wave signals (10kHz to 10MHz) from Agilent's arbitrary waveform generator M9330A. Then we applied our digital algorithm to improve SNR of acquired signals. The processed results are shown in Fig.4. From the graph, we could found that the best SNR of acquisition section approximately achieves 70dB. With the increasing of input signal's frequency, the total SNR of system will degrade slightly.

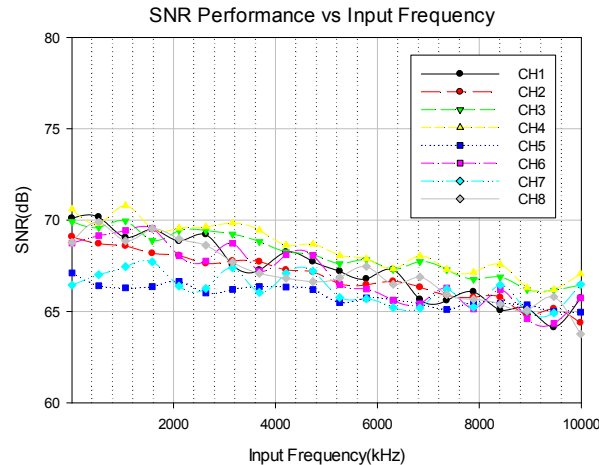


Figure 4. SNR Test Results

## Summary

For fulfill the high speed bioelectrical acquisition requirements in real-time applications, a novel high speed real-time acquisition system has been developed. System mainly consists of acquisition, distribution and storage section. By using 8 channel high-speed ADCs, advanced FPGA and solid-state storage technique, this system can acquire signal at high sample rate. The test results reveal the system has good SNR which above 70 dB.

## Acknowledgement

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