Fast and Accurate Dynamic Power Estimation method based on Component

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Abstract. Dynamic power optimization is an important part of the power optimization for embedded parallel processing. Dynamic power estimation is the premise for dynamic power optimization. The evaluation model with fast calculating speed and high accuracy can improve the efficiency for dynamic power optimization. The dynamic power evaluation methods based on low level simulation have high accuracy. But it is very time consuming. The high level dynamic power estimation models have higher speed, but have lower calculation accuracy. For this issue, the paper proposes a dynamic power estimation method based on component which combines ow level dynamic power evaluation methods with high level dynamic power estimation methods. The dynamic power of gray level co-occurrence matrix(GLCM) and fractal dimension(FD) in the remote sensing cloud detection based on texture feature is evaluated using the proposed method. The average error of the dynamic power for GLCM and FD is 11.86% using the proposed method. The computing time for GLCM and FD using the proposed method is 0.295 times than the method based XPower.

1 Introduction

Power consumption can be divided into dynamic power and static power. Dynamic power is the power producing by charging and discharging capacitance nodes in the circuit. The dynamic power is closely related with the implemented function and algorithm structure. Static power is mainly influenced by transistor size and junction temperature. The transistor size is decided by manufacture technology of FPGA, and the junction temperature is decided by working environment and manufacture technology of FPGA. Static power is independent of algorithm structure and computation complexity of the algorithm. So only the dynamic power can be optimized from algorithm level. While the dynamic power evaluation is the premise for dynamic power optimization. The evaluation model with fast calculating speed and high accuracy can improve the efficiency for dynamic power optimization.

The dynamic power evaluation methods based on low level simulation, such as XPower, have high accuracy[1][2]. But it is very time consuming. Because it could not get the dynamic power until finishing the synthesizing, placement and routing. For example, on the Pentium Dual-Core CPU E5300 platform, it needs 30-40 minutes to get the dynamic power when the resource consumption occupied 50% of the chip using ISE12.3 as the synthesized tool. It needs 60 minutes to get the dynamic power when the resource consumption occupied 80% of the chip. The high level dynamic power estimation models have higher speed[3][4]. Because of the feature of FPGA structure, the hardware structure of the application is very complexity. It is very difficult to propose a dynamic power model which is completely in conformity with the hardware structure. So the calculation accuracy of high level dynamic power estimation models is lower than the dynamic power evaluation methods based on low level simulation.

In tackling these questions, the paper proposes a dynamic power estimation method based on component which combines low level dynamic power evaluation methods with high level dynamic power estimation methods. The dynamic power of component is estimated by low level simulation. Then the dynamic power of the whole algorithm is estimated by high level estimation. Using this

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method can improve the calculating speed on the basis of promising the estimation accuracy.

2 The summary of dynamic power estimation method

The dynamic power of FPGA is the power generating by charging and discharging capacitance nodes in the circuit. The capacitance nodes include internal logic elements, routing resource et al. The following equation is used for estimating the dynamic power[5][6]:

$$P_{dyn} = \frac{1}{2} f \cdot V_{dd}^2 \sum_{i=1}^{N} C(i)F(i) \tag{1}$$

Where f is the clock frequency, V_{dd} is the power supply voltage, $C(i)$ is the load capacitance of the i[th] node, $F(i)$ (referred to as switching activity) is the average number of 0 to 1 transitions in one clock cycle.

Dynamic power estimation techniques for FPGA designs can roughly be divided into two categories[7-10]. One category is based on low level simulation, which is employed by tools such as PowerPlay from Altera, XPower from Xilinx et al. In order to estimate the dynamic power estimation based on low level simulation, simulation is performed to obtain the switching activity of the low level hardware components used in the FPGA design, such as the programming logic elements and the routing element.Using the low level simulation results, the dynamic power of the complete application is calculated. The creation of a low level implementation includes synthesis, placement and routing. This sequence forms a lengthy process. Simulations based on low level implementations are very time consuming.

The other category of dynamic power estimation is based on high level dynamic power models. The FPGA design is represented as a few high-level models interacting with each other. The high level models accept parameters that have a significant impact on dynamic power. These parameters are predefined or provided by the application designer. While dynamic power estimation using high level estimation can be fast, as they avoid time consuming low level simulation, its estimation accuracy varies among applications and application designers. One reason is that different applications demonstrate different dynamic power behaviors. In [8], it shows that using predefined parameters for dynamic power estimation results in estimation errors as high as 32% for input data with different statistical characteristics. The other reason is that requiring the application designer to provide these important parameters would demand a deep understanding of the energy behavior of the target devices and applications, which can prove to be very difficult in practice.

3 The dynamic power estimation based on component

Any applications(algorithm structures) can be decomposed to various components. The component is constructed by basic logic elements and routing resource and can implement a special function. So the dynamic power of component includes the dynamic power producing by the logic elements and the routing resource. In order to improve the calculation accuracy, a dynamic power estimation method based on component is proposed which combines low level simulation method with high level dynamic power estimation method.

Firstly, the application is divided into various components on the algorithm level. Secondly, the dynamic power of components with different parameters is got by low level simulation. Then curve fitting for one parameter and surface fitting for more than one parameter are used to get the component dynamic power. At last the total dynamic power is got by adding all components of the application. At the same time the component dynamic power is stored in the dynamic power library. It can be used for the other application dynamic power estimation.

3.1 the calculation of component dynamic power

The component dynamic power includes the dynamic power producing by the programming logic elements and the routing element. The programming logic elements are composed by Configurable Logic Block(CLB). The routing element is the routing resource which among the

programming logic elements. The dynamic power of the routing element depends on the length and the width of the routing and the switch activity.

After getting the simulation results of the component, the component dynamic power can be got by curve fitting or surface fitting. After getting the dynamic power function of one component, it can be used in any application which includes the component. There is no need to get the dynamic power using simulation.

In order to get the dynamic power function of component, component with different parameters would be simulated and the fitting method would be used according to the number of the parameters. Fig. 1 is flow chart of component dynamic power estimation.

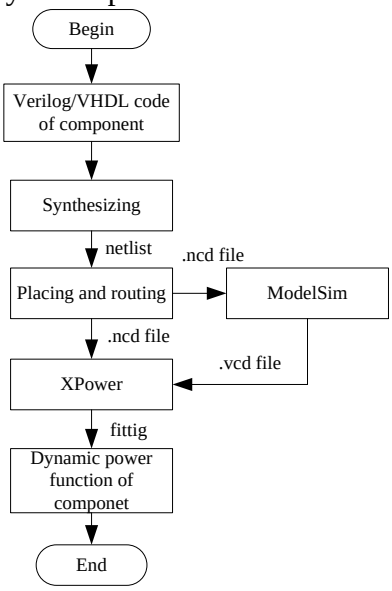

Fig. 1 flow chart of component dynamic power estimation

3.2 the total dynamic power calculation model

The total dynamic power is composed by the component dynamic power. So the accumulating the dynamic power of all components can get the total dynamic power. The following formula is used for estimating the dynamic power of the application:

$$P = \sum_{i=1}^{k} \sum_{j=1}^{n_i} P_{ij} \tag{4.28}$$

Where k is species quantity of the component, n_i is the number of the i^{th} component, $i = 1, 2, ..., k$, P_{ij} is the j^{th} component dynamic power of the i^{th} specie. In order to convenient calculation, the component dynamic power in any place of the FPGA is assumed the same. Fig. 2 is flow chart of the total dynamic power.

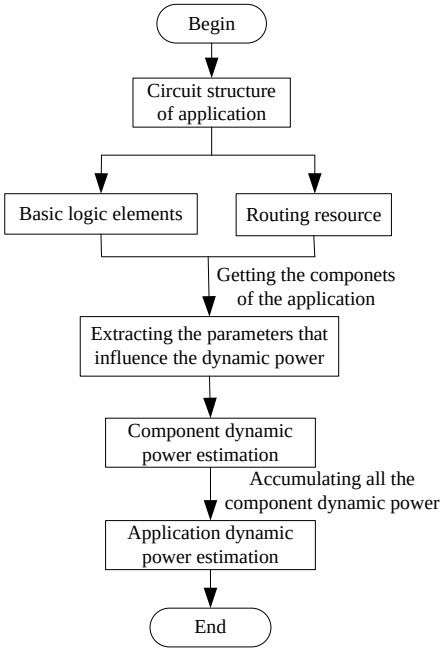

Fig. 2 flow chart of the total dynamic power

4 Method validation and experimental result analysis

In order to validate the efficiency of the proposed method, using this method to evaluate the dynamic power of gray level co-occurrence matrix(GLCM) and fractal dimension(FD) in the remote sensing cloud detection based on texture feature[11]. The calculation accuracy and computing time are compared with the dynamic power estimation methods that have been proposed.

4.1 dynamic power estimation

According to the calculation characteristics of the cloud detection based on texture feature, multi-PE parallel method can be used to calculate the GLCM and FD[12]. Fig. 3 and Fig. 4 are the PE structures for GLCM and FD respectively.

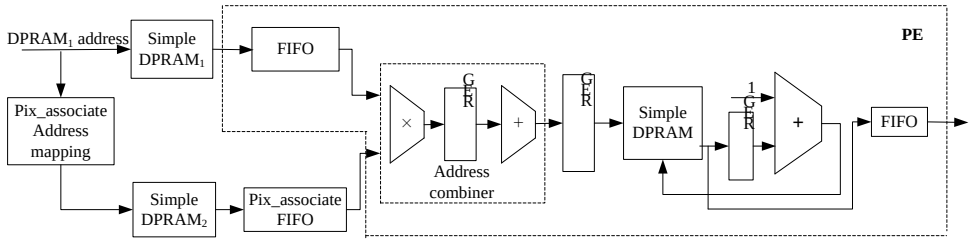

Fig. 3 The PE structure for GLCM calculation

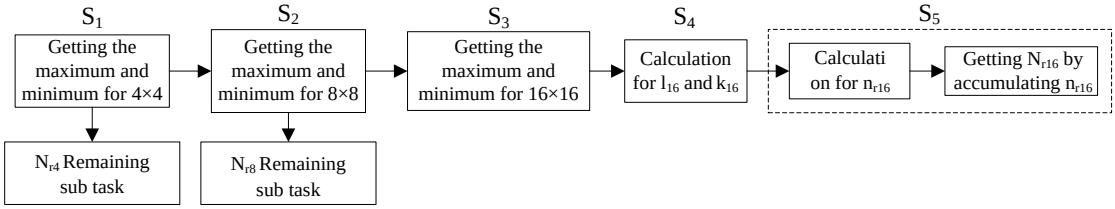

Fig. 4 The PE structure for FD calculation

In order to fully consider the influence of routing resource to dynamic power and improve the calculation accuracy, single PE is used as the component to estimate the dynamic power. Elements influencing the component dynamic power include clock frequency(f), word length(M) and the power supply voltage. Because the remote sensing image is gray image and the maximum gray level is 256, the word length of the input data is 8. And the power supply voltage keeps invariant.

So f is the only element that influences the component dynamic power estimation of GLCM and FD. Formula 3 and 4 are the component dynamic power for GLCM and FD.

$$P_{GLCM\_PE}(f) = 0.773f - 15.741 \tag{3}$$

$$P_{FD\_PE}(f) = 2.761f + 0.995 \tag{4}$$

The total dynamic power can be got according to formula 5 and 6. Where n_{PE_GLCM} and n_{PE_FD} are the component number of calculating GLCM and FD respectively.

$$P_{GLCM} = n_{PE\_GLCM} \times P_{GLCM\_PE}(f) \tag{5}$$

$$P_{FD} = n_{PE\_FD} \times P_{FD\_PE}(f) \tag{6}$$

4.2 experimental result analysis

The input image size is 64×64 and the maximum gray level of the image is 256. The hardware platform of the experiment is Virtex V XC5VFX100T. The clock frequency is 60MHz. In the experiment, the .ncd file is produced by ISE12.3 and the .vcd file is produced by ModelSim se 6.5e. The component dynamic power can be calculated when the .ncd file and the .vcd file are input to the XPower. Four PEs are used to calculate the GLCM and FD respectively in the experiment.

(1) Calculation accuracy comparison and analysis

Table 1 shows the dynamic power comparison of different methods. The dynamic power got by XPower is used as the reference power. The average error of the dynamic power for GLCM and FD is 9.66% using the method in [10].The average error of the dynamic power for GLCM and FD is 11.86% using the proposed method. The dynamic power is smaller than real dynamic power and the dynamic power calculated by [10], that is because the dynamic power generating by routing resource among PEs is neglected in the proposed method.

Table 1 the dynamic power comparison of different methods

	Method based on XPower	The method in [10]	The proposed method
Dynamic power for GLCM(mW)	128.37	116.07	112.72
Error of dynamic power for GLCM	0%	9.58%	12.19%
Dynamic power for FD(mW)	175.95	158.83	155.66
Error of dynamic power for FD	0%	9.73%	11.53%

(2) Computing time comparison and analysis

Table 2 shows the computing time for calculating dynamic power of different methods. The computing time for GLCM using the proposed method is 0.27 times than the method based XPower and is 0.35 times than the method in [10]. The computing time for FD using the proposed method is 0.32 times than the method based XPower and is 0.37 times than the method in [10].

Table 2 Computing time for calculating dynamic power of different methods

	Method based on XPower	The method in [10]	The proposed method
Computing time for GLCM(min)	30.2	23.4	8.3
Computing time for FD(min)	42.4	36.9	13.5

Analysis indicated that calculation accuracy of the proposed method is decreased than the other method. However the computing time of the proposed method is improved greatly. If the calculation accuracy within permissible error range, the proposed dynamic power method can efficiently improve the estimation efficiency.

5. Conclusion

The paper proposes a dynamic power estimation method based on component which combines dynamic power evaluation methods based on low level simulation with high level dynamic power estimation methods. The dynamic power of component is estimated by low level simulation. Then the dynamic power of the whole algorithm is estimated by high level estimation. In order to validate the method, the dynamic power of GLCM and FD is evaluated using the proposed method. Experimental results indicate that the method has higher speed on the premise of without decreasing the calculation accuracy.

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References

[1] R Jevtic, C Carreras. Power Measurement Methodology for FPGA Devices[J]. IEEE Transactions on Instrumentation and Measurement, 2011, 60(1): 237-247.

[2] B Pandey, J Yadav, Y K Singh et al. Energy Efficient Eesign and Implementation of ALU on 40nm FPGA[C]. 2013 International Conference on Energy Efficient Technologies for Sustainability, 2013: 45-50.

[3] S M Afifi, F Verdier, C Belleudy. Power Estimation Method Based on Real Measurements for Processor-Based Designs on FPGA[C]. 2014 International Conference Computational Science and Computational Intelligence, 2014, 260-263.

[4] H Hajimiri, K Rahmani, P Mishra. Efficient Peak Power Estimation Using Probabilistic Cost-Benefit Analysis[C]. 2015 28th International Conference on VLSI Design, 2015, 369-374

[5] A P Chandrakasan, S Sheng, R W Brodersen. Low power CMOS Digital Design[J]. IEEE Journal of Solid State Circuits, 1992, 27(4): 473-484.

[6] R Basmadjian, H Meer. Evaluating and Modeling Power Consumption of Multi-core Processors[C]. 2012 Third International Conference on Future Energy Systems: Where Energy, Computing and Communication Meet, 2012: 1-10.

[7] Xiaoyu Ni, Teng Wang, Yueming Zhao. System-Level Power Estimation with On-Chip Bus Performance Monitoring Units in PKU-DSPII SoC[C]. 2012 IEEE 12th International Conference on Computer and Information Technology, 2012: 119-123.

[8] J Ou, K prasanna. PyGen: a MATLAB/Simulink Based Tool for Synthesizing Parameterized and Energy Efficient Designs using FPGAs[C]. The 12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 2004: 47-56.

[9] S Bilavarn, G Gogniat, J L Philippe et al. Design Space Pruning through Early Estimations of Area/Delay Trade-offs for FPGA Implementations[J]. IEEE Transactions on Computer Aided Design, 2006, 25(10): 1950-1968.

[10] R Jevtic, C Carreras. A Complete Dynamic Power Estimation Model for Data-paths in FPGA DSP Designs[J]. Integration, the VLSI Journal, 2012, 45(1): 172-185.

[11] Q Cao, H Zheng, X S Li. A method for detecting cloud in satellite remote sensing image based on texture[J]. Acta Aeronautica et Astronautica Sinica, 2007, 28(3): 661-666.

[12] H Zheng, Z Li, J Li. Fast Implementation and Optimal Method of Gray Level Co-occurrence Matrix[J]. Chinese Journal of Scientific Instrument, 2012, 33(11): 2509-2515.