

## An Ultra-low-power Integrated RF Front-end Based on Chip Transformer for UWB system

Yi Li, Chunhua Wang, Kui Fu

College of Information Science and Engineering, Hunan University, Changsha 410082,  
P.R.China

Email:wch1227164@hnu.edu.cn

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**Abstract.** In this paper, an ultra-low-power integrated RF front-end for UWB system is proposed. It contains a single-ended low noise amplifier (LNA) and a double balanced mixer. The resistive shunt feedback topology is employed to achieve a good input impedance matching in the whole UWB band. The stacked common-source (CS) LNA is adopting current-reuse and forward body bias techniques to reduce working current and voltage considerably. A transformer network is employed between LNA and double balanced mixer, which not just helps to convert the single-ended signal to differential signal, but also makes a great contribution to save the power consumption of the front-end circuit. Fabricated in the TSMC 0.18- $\mu\text{m}$  RF CMOS technology, the  $S_{11}$  of the front-end is below -10dB in 3.1~10.6GHz. It achieves a conversion gain of 18.3~20.5dB, the double sideband (DSB) NF of 4.3~6.1dB. The IIP3 are -3.8dBm at 4.5GH. It consumes 2.4mA from a 0.8V supply voltage and occupies an active area of only 0.86\*0.52 mm<sup>2</sup>.

### Introduction

Ultra-wideband (UWB) technology has attracted great interest in both academia and industry in recent years for short range and high speed wireless communication systems. Recent developments have resulted in the development of CMOS radio frequency integrated circuits (RFICs) for UWB receivers. The receivers' gain and noise characteristics are closely related to the system sensitivity and dynamic range. However, it usually requires considerable power to boost the transistor performance. Therefore, many UWB receivers were developed at the expense of power consumption [1-3]. LNA and mixer are critical blocks in a UWB receiver. LNA usually determines the system NF and gain. This paper will propose an integrated ultra-low-power front-end circuit for UWB receivers.

There have been several reported implementations of low power RFICs in the last few years [4-11]. Although these circuits' power consumption aren't low enough for satisfying the target of ultra-low-power RFICs, the techniques adopted by these researches to lower power still have significance for ultra-low-power RFICs. For ultra-low-power design of single module circuit, the most efficient technological method of reducing power consumption is to reduce supply voltage or current. Therefore, many effective techniques are adopted to achieve the aim. For example, folded cascade structure has been used in reference [8] to reduce the supply voltage, but it induced more branch current. Reference [9] introduced the subthreshold technique, which make the transistor work in a weak inversion region and reduce the supply voltage down to 0.6V. However, the subthreshold technique induced gain and NF performances degradation [10]. Recently, current-reuse topology and forward body bias technique are used to lower power consumption for RFICs [4, 10-11]. However, few researchers concentrate on the design of ultra-low-power LNA for multi-standard receivers, especially for UWB systems.

In this work, the front-end circuit adopts a resistive shunt feedback topology and a parallel LC load to achieve wideband input impedance matching in 3.1~10.6GHz [12]. Furthermore, the LNA reduces its power consumption by incorporating the current-reuse with forward body bias

techniques. To realize the monolithic integration between single-balanced LNA and double-balanced mixer, the on-chip transformer is introduced. It not only helps to convert the single-ended signal to differential signal, but also makes a great contribution to save the power consumption of the front-end circuit. Finally, the proposed circuit achieves a good performance over the whole UWB band range from 3.1 to 10.6GHz while the power consumption is extremely low.

### Circuit Implementation

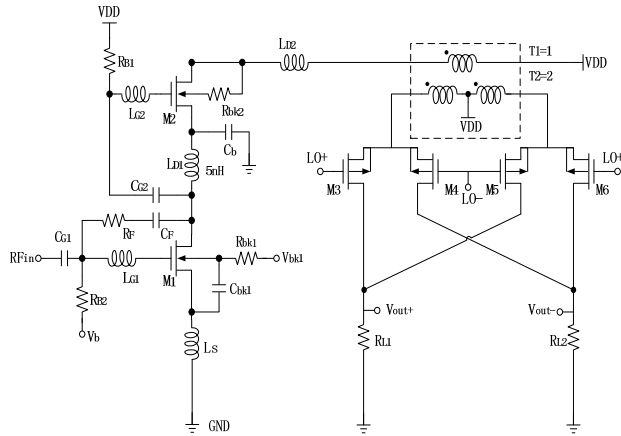


Fig. 1 Proposed ultra-low-power UWB receiver front-end circuit.

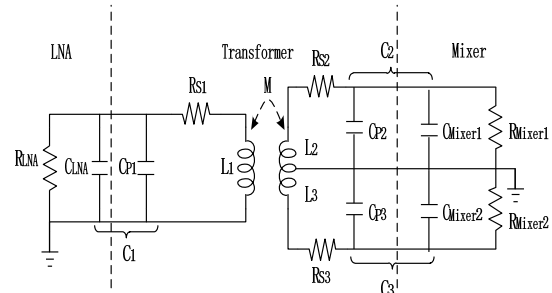


Fig. 3 The equivalent circuit based on transformer model.

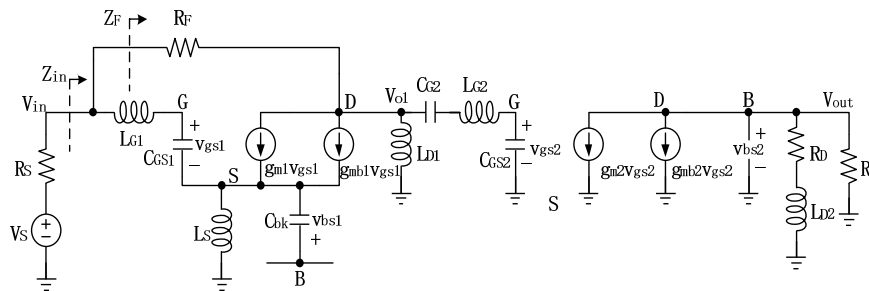


Fig. 2 Small-signal equivalent circuit of the LNA part.

The proposed integrated ultra-low-power RF front-end for 3.1~10.6GHz UWB system is shown in Fig. 1, the input stage was designed by employing a resistive shunt feedback topology together with a parallel LC load to match to a 50Ω antenna. For flexibility of the design, a source degeneration inductor  $L_S$  is placed in series with the source. The stacked structure of amplifying circuit is adopted to save more branch current. Moreover, current-reuse configuration is applied to the 2-stage cascade common source LNA. The signal amplified by  $M_1$  is coupled to the gate of  $M_2$  by  $C_{G2}$  while the source of  $M_2$  is bypassed by  $C_b$ . Besides, forward body bias technique is applied to reduce the supply voltage of LNA. By adding a positive voltage  $V_{bk1}$  and a current limiting resistor  $R_{bk1}$  to body terminal of  $M_1$ , forward body bias architecture of  $M_1$  is formed. The forward body bias voltage of  $M_2$  is directly obtained from the drain of  $M_2$ , which helps to simplify the structure of bias circuit. With  $M_1$  and  $M_2$  sharing the same bias current and working at a low supply voltage, the power consumption of LNA is minimized. Moreover, the inductive load  $L_{D1}$  and  $L_{D2}$  of 1st and the 2nd amplifier stage help to achieve a high power gain, and the supply voltage won't be influenced since the voltage drop across them is negligible. A peaking inductor  $L_{G2}$  is added to the gate of  $M_2$  to double the 3dB bandwidth of the output stage, so the high frequency poles of the LNA can be pushed outside of the 3.1~10.6GHz band of interest.

To implement further low power design, an on-chip transformer is employed between LNA and mixer to convert the single-ended signal to differential signal, while it also provides current gain for the front-end circuit. The equivalent circuit based on transformer model is shown in Fig. 3. Where  $C_{P1}$ ,  $C_{P2}$ ,  $C_{P3}$ ,  $R_{S1}$ ,  $R_{S2}$  are the parasitic parameters caused by on-chip transformer.  $R_{LNA}$ ,  $C_{LNA}$  is the output impedance parameter of the LNA.  $R_{Mixer}$ ,  $C_{Mixer}$  is the input impedance parameter of the mixer. Resonator  $L_1-C_1$  is connected to the output of LNA, resonators  $L_2-C_2$  and  $L_3-C_3$  are connected to the mixer input using a center-tapped coil.

The current signal is transferred from  $L_1-C_1$  to  $L_2-C_2$  and  $L_3-C_3$  through the magnetic coupling in the transformer. In this process, its contribution for saving power consumption as follows: First, it converts single-ended signal to differential signal without any power consumption, because the transformer consists of passive component. Usually, the traditional single to differential circuit consists of active transistors, which consume power. Second, the transformer directly injects current signal to the switching stage of mixer, which helps mixer save the power consumption of transconductance stage. Finally, the mixer become a single layer transistor structure while the transconductance stage it omitted, which make it work under a lower supply voltage and save more power. Therefore, the on-chip transformer make a momentous contribution for saving the power consumption.

### Input Matching

The complete small signal equivalent circuit of the LNA part is shown in Fig. 2. Due to the forward body bias technique is applied to the NMOS transistors, the back-gate transconductance ( $g_{mb}$ ) of them shouldn't be ignored and it can be analyzed as followed:

$$g_{mb} = (\eta - 1)g_m \quad (1)$$

$$\eta = 1 + \frac{\gamma}{2\sqrt{2}|\phi_f| - V_{bs}} \quad (2)$$

In the type  $g_m$  is the transconductance of the NMOS transistor.  $V_{bs}$  of the transistor increases, then  $\eta$  and  $g_{mb}$  increases, which has an influence on the following analysis. Considering the effect of the back-gate transconductance ( $g_{mb}$ ) caused by forward body bias technique, the input impedance is as Eq. (3):

$$Z_{in} = \left[ S(L_{g1} + L_S) + \frac{1}{SC_{gs1}} + \frac{(g_{m1} + g_{mb1})L_S}{C_{gs1}} \right] // Z_F \quad (3)$$

In the type  $g_{m1}$  and  $g_{mb1}$  are the transconductance and back-gate transconductance of  $M_1$ ,  $Z_F$  is the impedance looking into the shunt resistive feedback, and can be given as:

$$Z_F = \frac{R_F + (SL_L // \frac{1}{SC_L})}{1 + \frac{g_{m1} + g_{mb1}}{S^2 C_{gs1} (L_{g1} + L_S) + S(g_{m1} + g_{mb1})L_S + 1} \cdot \left( SL_L // \frac{1}{SC_L} \right)} \quad (4)$$

The input matching bandwidth decreases with the increasing of  $R_F$ , but the value of  $R_F$  has an effect on the NF. There is a tradeoff between input matching bandwidth and NF when  $R_F=400\Omega$ , and other parameters used as follows:  $L_{G1}=1.43\text{nH}$ ,  $L_S=0.1\text{nH}$ ,  $C_F=3.5\text{pF}$ ,  $C_{G2}=0.58\text{pF}$ ,  $L_{G2}=1.1\text{nH}$ ,  $L_{D1}=2.44\text{nH}$ ,  $C_b=3.3\text{pF}$ .

## Noise Analysis

The noise figure of the first stage is critical to the whole circuit. The noise factor of the first stage is as follows:

$$F \approx 1 + \frac{R_G + R_{LG1} + R_{SS} + R_{LS}}{R_S} + \frac{\delta\alpha\omega^2 C_{gs1}^2 R_S}{5(g_{m1} + g_{mb1})} + \frac{R_F [(L_{G1} + L_S) C_{gs1}]^2}{R_S [(g_{m1} + g_{mb1}) R_F - 1]^2} \cdot \left| S^2 + S \left( \frac{\omega_{0,RF}}{Q_{RF}} \right) + \omega_{0,RF}^2 \right|^2 + \frac{\gamma(g_{m1} + g_{mb1})(R_F + R_S)^2 \cdot [(L_{G1} + L_S) C_{gs1}]^2}{\alpha R_S [(g_{m1} + g_{mb1}) R_F - 1]^2} \cdot \left| S^2 + S \left( \frac{\omega_{0,D}}{Q_D} \right) + \omega_{0,D}^2 \right|^2 \quad (5)$$

In the type(5)

$$\omega_{0,RF} = \sqrt{\frac{1 + (g_{m1} + g_{mb1}) R_S}{(L_{G1} + L_S) C_{gs1}}} \quad (6)$$

$$\omega_{0,D} = \frac{1}{\sqrt{(L_{G1} + L_S) C_{gs1}}} \quad (7)$$

$$Q_{RF} = \frac{C_{gs1}}{R_S C_{gs1} + (g_{m1} + g_{mb1}) L_S} \sqrt{\frac{(1 + g_{m1} + g_{mb1})(L_{G1} + L_S)}{C_{gs1}}} \quad (8)$$

$$Q_D = \frac{C_{gs1}}{(R_F // R_S) C_{gs1} + (g_{m1} + g_{mb1}) L_S} \sqrt{\frac{L_{G1} + L_S}{C_{gs1}}} \quad (9)$$

In the type(5),  $R_G$ ,  $R_{SS}$  represent the thermal noise induced by gate and source resistors of M1.  $R_{LG1}$ ,  $R_{LS}$  are the thermal noise caused by  $L_{G1}$  and  $L_S$  while working at high frequencies. From Eq. (5), since  $NF=10\log_{10}F$  has been put in the form of a second order function of  $S$ , its frequency response is controlled by  $Q$  factors  $Q_{RF}$  and  $Q_D$ . However, from Eq. (8) and Eq. (9),  $Q_{RF}$  and  $Q_D$  is mainly impacted by the value of  $L_S$  and  $R_F$ , so we can decrease the NF by choosing suitable value of  $L_S$  and  $R_F$ .

## Gain Analysis

The conversion gain of the front-end circuit is provided by the first stage, second stage of LNA and the transformer network. The body effects and parasitic capacitances are not considered. The voltage gain of the first stage of LNA can be expressed as Eq. (10):

$$A_1 = \frac{V_{o1}}{V_{in}} = - \left( R_F // SL_L // \frac{1}{SC_L} \right) \cdot \left( g_{m1}' - \frac{1}{R_F} \right) \quad (10)$$

$$g_{m1}' = \frac{g_{m1} + g_{mb1}}{S^2 C_{gs1} (L_{G1} + L_S) + S(g_{m1} + g_{mb1}) L_S + 1} \quad (11)$$

The voltage gain of the second stage of LNA is given by:

$$A_2 = \frac{V_{out}}{V_{o1}} = -(g_{m2} + g_{mb2}) \left[ R_b // (R_D + SL_{D2}) \right] \cdot \frac{1}{S^2 L_{G2} C_{gs2} + \left( 1 + \frac{C_{gs2}}{C_{G2}} \right)} \approx -(g_{m2} + g_{mb2}) \cdot (R_D + SL_{D2}) \quad (12)$$

In the type  $g_{m2}$  and  $g_{mb2}$  are the transconductance and back-gate transconductance of  $M_2$ . The gain increases with the increasing of  $R_D$ , but too large  $R_D$  worsens output matching. Therefore,  $L_{D1}$  and  $L_{D2}$  are adopted to improve the gain at high frequencies. However, we can increase  $g_{m1}$  and  $g_{m2}$  to compensate the degradation of gain, but it will cause larger power consumption, so the tradeoff between gain and power should be considered. In this paper  $g_{m1}=24\text{ms}$ ,  $g_{m2}=27\text{ms}$ .

The on-chip transformer provides a current gain by impedance transformation. The close form of the transformer network current gain can be derived as

$$\frac{i_{out}}{i_{in}} = \frac{-j2kQ\omega_n}{\left\{ \omega_n \left[ 1 + jQ \left( \omega_n - \frac{1}{\omega_n} \right) \right] \right\}^2 + (kQ)^2} \cdot \frac{1}{2} \sqrt{\frac{R_s}{R_L}} \quad (13)$$

where

$$Q \equiv R_s C_1 \omega_o = R_L C_2 \omega_o \quad (14)$$

$$\omega_o \equiv \frac{1}{\sqrt{L_1 C_1 (1-k^2)}} = \frac{1}{\sqrt{L_2 C_2 (1-k^2)}} \quad (15)$$

In the type k is the coupling coefficient, which is determined by the mutual inductance between the two coils of the on-chip transformer. In this design, an ideal transformer model has been employed to supply a current gain, and the coupling coefficient  $k=0.5$ .

## Simulation Results

The RF receiver front-end is implemented in TSMC 0.18- $\mu\text{m}$  CMOS technology. The receivers' supply voltage falls to 0.8V when the forward body bias voltages are chosen at  $V_{bkl}=0.44\text{V}$ . Operating in 3.1GHz~10.6GHz, the input reflection coefficient  $S_{11}$  are respective less than -10dB which is shown in Fig. 4. The double sideband NF are 4.3~6.1dB as shown in Fig. 5. In Fig. 6, the conversion gain are 18.3~20.5dB. As shown in Fig. 7, the IIP3 of the front-end is -3.8dBm at 4.5GHz. The layout of the front-end is shown in Fig. 8, occupying  $0.86 \times 0.52\text{mm}^2$  active area. The power consumption is only 1.9mW, which is far below the same applied RFICs. Tab. 1 summarizes the performance of the proposed front-end and compares the recently reported UWB front-end. Our proposed front-end achieves an acceptable NF and linearity performances under ultra-low-power consumption..

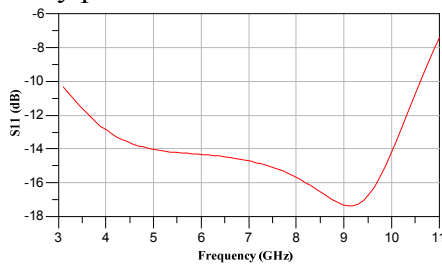


Fig. 4 Simulation of  $S_{11}$  parameter of the front-end

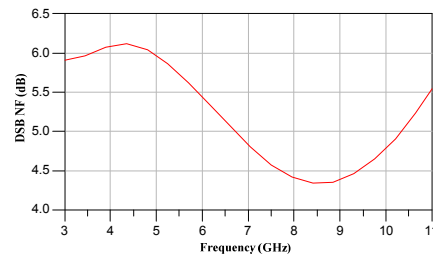


Fig. 5 Simulation of double sideband NF of the front-end

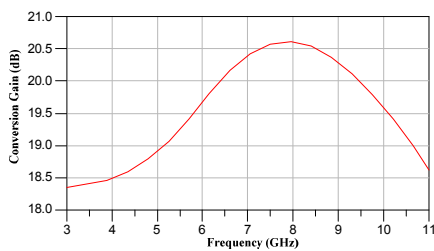


Fig. 6 Simulation of conversion gain of the front-end

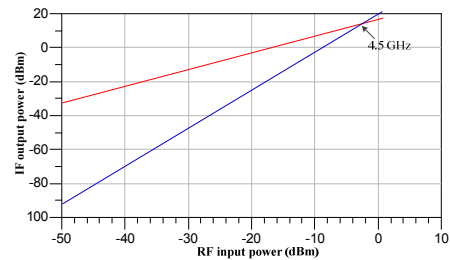


Fig. 7 Simulation of the IIP3 of the front-end

Reference <sup>o</sup>	[1] <sup>o</sup>	[2] <sup>o</sup>	[3] <sup>o</sup>	[12] <sup>o</sup>	This Work <sup>o</sup>
BW (GHz) <sup>o</sup>	3.1 ~ 10.6 <sup>o</sup>	3 ~ 8.5 <sup>o</sup>	3.1 ~ 10.6 <sup>o</sup>	3.1 ~ 10.6 <sup>o</sup>	3.1 ~ 10.6 <sup>o</sup>
NF (dB) <sup>o</sup>	2.8 ~ 3.4 <sup>o</sup>	3.1 ~ 4.4 <sup>o</sup>	4.5 ~ 5 <sup>o</sup>	3.74 ~ 4.74 <sup>o</sup>	4.3~6.1 <sup>o</sup>
$S_{11}$ (dB) <sup>o</sup>	< -9.7 <sup>o</sup>	< -11.5 <sup>o</sup>	< -10.5 <sup>o</sup>	< -8.6 <sup>o</sup>	< -10 <sup>o</sup>
Gain (dB) <sup>o</sup>	11.0 ~ 11.8 <sup>o</sup>	16.0 <sup>o</sup>	14.5 <sup>o</sup>	11.63 ~ 12.89 <sup>o</sup>	18.3~20.5 <sup>o</sup>
IIP3 (dBm) <sup>o</sup>	0.72 <sup>o</sup>	-5.4 <sup>o</sup>	-4.8 <sup>o</sup>	-4 <sup>o</sup>	-3.8 <sup>o</sup>
Supply (V) <sup>o</sup>	1.9 <sup>o</sup>	1.2 <sup>o</sup>	1 <sup>o</sup>	1.8 <sup>o</sup>	0.8 <sup>o</sup>
Power (mW) <sup>o</sup>	22.7 <sup>o</sup>	16 <sup>o</sup>	7 <sup>o</sup>	10.34 <sup>o</sup>	1.9 <sup>o</sup>
Technology <sup>o</sup>	0.18 $\mu\text{m}$ <sup>o</sup>	90nm <sup>o</sup>	0.18 $\mu\text{m}$ <sup>o</sup>	0.13 $\mu\text{m}$ <sup>o</sup>	0.18 $\mu\text{m}$ <sup>o</sup>

Tab. 1: Performance Summary of The Recently Reported UWB Front-end

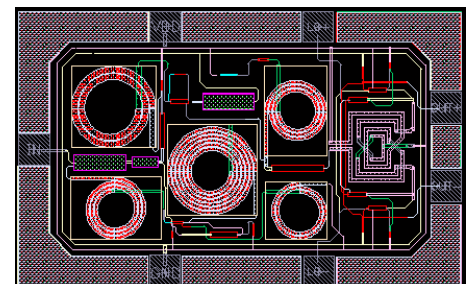


Fig. 8 Layout of the RF receiver front-end

## Conclusion

This paper describes the design of an ultra-low-power RF front-end for UWB system. By employing transformer network and other power optimizing techniques, the total measured conversion gain of the receiver is 18.3~20.5dB and DSB NF is 4.3~6.1dB. The IIP3 are -3.8dBm at 4.5GHz. All of these results satisfy the requirements of the UWB receiver. Especially, the power consumption of the circuit is 1.9mW with a 0.8V supply voltage, which meets the demand for ultra-low-power applications.

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## About Authors

**Yi Li He** is currently studying in Hunan University for Ph.D. degree. His research interests include mobile communication network plan & optimization, RF design with focus on multi-mode receiver. E-mail: wch1227164@hnu.edu.cn