A 6GHz Input Bandwidth Track-and-Hold circuit in HBT Technology

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Abstract. This paper presents the design of a 6GHz track-and hold circuit with input bandwidth. The track-and hold circuit adopts the design simulation of HBT process, able to work at a sampling frequency of 2 GHz, the highest sampling frequency can reach about 2 GHz. The SFDR of the track-and hold circuit can reach 64dB (simulation work at 2 GHz),The track-and hold circuit provides more than 66 dB hold –mode SFDR3 for 0 to 2GHz 1Vpp input signals at 2GHz. Early product parameters of the track-and hold circuit (working in 2 GHz sampling frequency) are as follows: the SFDR parameter can be achieved 64 dB.

Introduction

Wideband data acquisition systems with multi-GHz bandwidth are needed for a variety of applications such as software defined radio, radar systems, and test and measurement equipment. The track and hold circuit is usually used in the front end of A/ D converter to complete the tracking of the input signal, and he plays a vital role in the performance of the whole converter. Ultra wideband sampling and holding circuit can realize the receiving and conversion of wide band input signal, and achieve good linearity in the whole wide band. Thus, the application of the A/D converter is flexible and convenient and the circuit system is stable and reliable. Ideally, system designers would like to be able to connect the signal source (for example an antenna) directly to a wideband, high dynamic range Analog-to-Digital Converter (ADC) for digitization. Although few of high speed ADCs offer input bandwidth beyond a few GHz. In addition, maintenance of good sampling linearity is technologically challenging and most current ADCs suffer rapidly degrading linearity above 1 or 2 GHz signal frequency [1,2,3,5,6,7].

A design and measurements of the track-and-hold circuit in heterojunction bipolar transistor （HBT） technology which has 2 GHz input bandwidth and mainly intended to be used in the ADC is described in this paper.

Design of the Circuit

While the track and hold circuit is received by the signal, the input signal is sampled and hold, and the basic working state can include the sampling period and the holding stage. At the sampling stage, the circuit is sampled and tracked, and the output signal is directly followed by the input signal. In the holding phase, the circuit will turn off the input signal and output the tracking state to maintain the input signal information and hold the status signal until the end of the command. Figure 1 is a diagram of the working principle of the track and hold circuit.

The track and hold circuit design includes the function modules such as the core of track-and-hold circuit, input signal buffer circuit, output signal buffer circuit, sampling clock input circuit，the bias circuit and so on. The input signal buffer circuit is used to improve the input impedance of the whole circuit, and the output signal buffer circuit is used to reduce the output impedance of the circuit, so that the signal source and the load link can be matched. The sampling clock input buffer circuit receives the clock, and after the processing, directly to the core of

track-and-hold circuit, control the work of the track and hold circuit. The input signal is processed by the input buffer circuit. Figure 2 is a block diagram of the track and hold circuit.

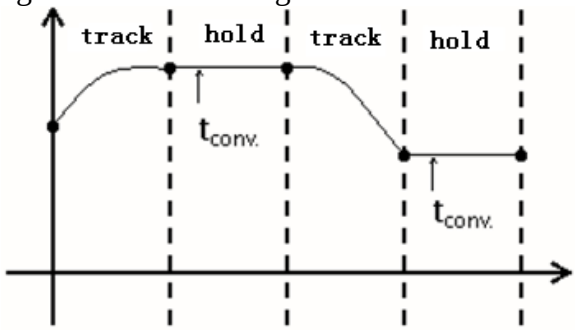


Fig.1. working diagram of the track and hold circuit

In the circuit design, the circuit supply include positive power supply, negative power supply, reference point for design, in which the negative power supply design is 3.3V, the power supply is designed for 2V, the reference point for 0V. Circuit supply is divided into the power of the clock and the signal power supply area of the design, the input signal and the input clock can play a certain role in isolation. Detailed circuit unit design is as follows.

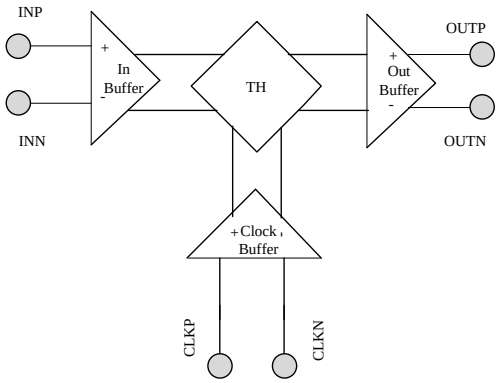


Fig.2. principle diagram of the track and hold circuit.

A. Input Buffer unit

Due to the high sampling frequency of the circuit, in order to receive the input signal effectively and ensure the input signal bandwidth, the input signal buffer circuit is designed. Figure 3 is a specific input buffer circuit.

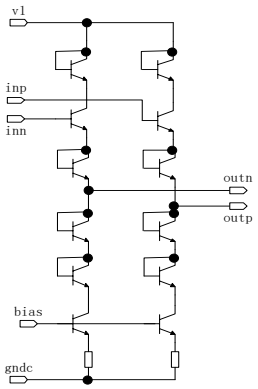


Fig.3. Input buffer circuit diagram

Shown in Fig.3, the input buffer unit is mainly composed of HBT transistors and resistors, mainly to complete the input signal of the receiving, and the input signal is buffered output, thereby increasing the ability of driving signal. The circuit uses the ECL emitter follower architecture circuit to design, better to achieve the matching between the input signal and the level of the sampling circuit, but also to protect the bandwidth of the input signal.

B. Output Buffer unit

After sampling, the signal can not be directly output driving circuit, in order to drive the

follow-up circuit, the signal is amplified and output design, so as to improve the driving ability of the sampled signal. Figure 4 is the output signal buffer circuit.

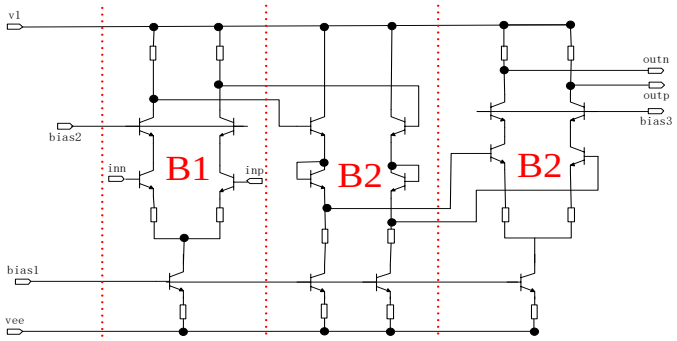


Fig.4. Ouput buffer circuit diagram

From the circuit diagram shown in Figure 4 it can be seen that the output buffer circuit is composed of three stages: B1, B2, B3. B1 is the first buffer amplifier, and the signal output bandwidth is set up, the output signal bandwidth of this level circuit is designed to be 2GHz, which can suppress the high frequency signal of the input tracking state, thus achieving the processing capability of the high input bandwidth signal to 2GHz. B2 is designed as the second stage, which can be used to isolate the first and the third pole, while the signal is transferred to the third pole from the first level. B3 as the output circuit of the third pole of the output signal to achieve the driving ability to improve, while the output impedance of 50 ohm matching, easy to use products.

C. Bias unit

Shown in Fig.5, the bias unit main generates a bias voltage. The bias circuit is designed by HBT device, which provides the bias voltage for the whole circuit, and has a good matching with the constant current source circuit structure and can realize the temperature stability and reliability of the whole circuit.

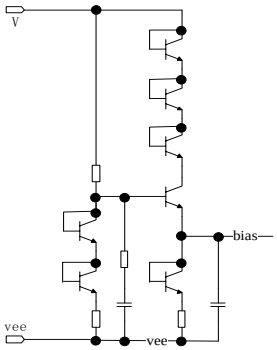


Fig.5. the bias circuit

D. Input clock buffer

The input clock buffer circuit mainly realizes the receiving of the high speed clock, and improves the signal driving ability while achieving the level matching, and finally realizes the control of the working state of the sample and hold circuit. Figure 6 is the input clock buffer circuit.

From the circuit diagram shown in Figure 6, the input clock buffer circuit receives the input signal, and the signal amplitude of the input clock signal is amplified, which can ensure the requirement of the track and hold circuit core, and also realize the low driving ability of the input clock signal.

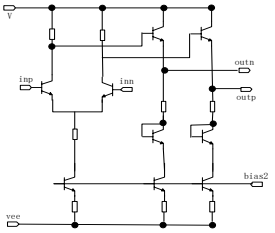


Fig.6. Input clock buffer circuit diagram

E. The core of track-and-hold circuit

The core of track-and-hold circuit is the core part of the whole track and hold circuit. The circuit is applied to the structure of the fully differential switch emitter follower (SEF), which is the common structure of the track and hold circuit design using HBT. The simplified circuit diagram of the core is shown in Figure 7, it mainly includes the design of sampling switch, output emitter follower.

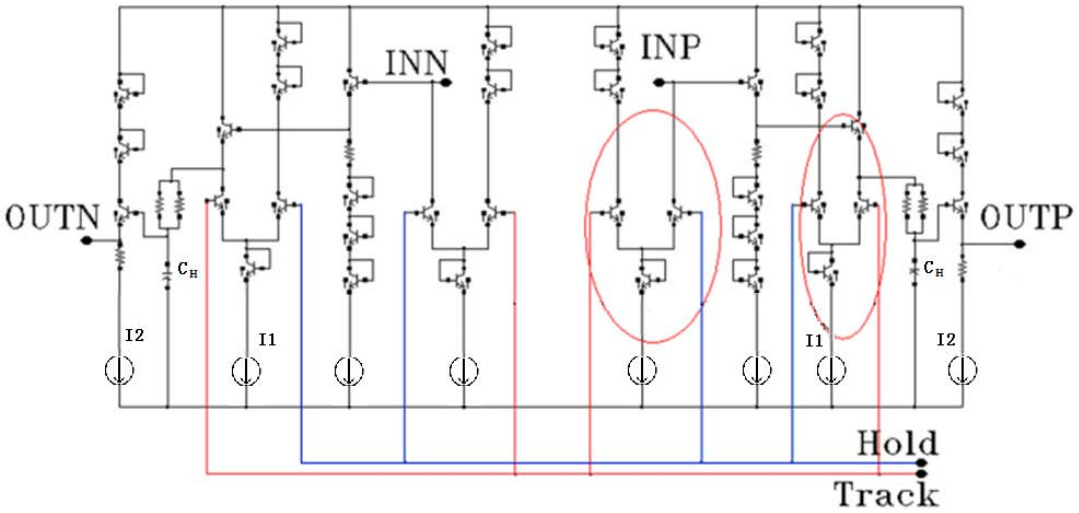


Fig.7. Input clock buffer circuit diagram

From Figure 7 shows the circuit diagram can be seen, the input clock directly control the working state of the circuit. When the hold state is high effective, the clock control circuit of the fully differential operation is in the holding state and the input signal is turned off, and the signal is hold on the capacitor (C_H). When the Track state is high, the clock control circuit of the fully differential operation is in the tracking state and the input signal is turned on, the emitter follower directly outputs the input signal. The key of circuit design is the design of I_1 and C_H, which directly determines the maximum working bandwidth of the track and hold circuit, The f_{IN_MAX} can be expressed as (1).

$$f_{IN\_MAX} = \frac{I_1}{\pi \bullet C_H \bullet A_{IN}} \tag{1}$$

In the core of track-and-hold circuit, I_1 is 1.25 mA and A_{IN} is 1Vpp ,so the design value of f_{IN} is more than 6GHz[4]。In the practical work, we also need to consider the influence of various parasitic effects, processing technology and other factors, in order to ensure the design of the circuit.

After the completion of the circuit design of each function module, according to the diagram of track-and-hold circuits on the circuit of the overall design。In addition, the layout of the circuit was designed and processed. In the layout design of the circuit, the design of the input and output interface needs the impedance matching design, the bandwidth allocation design, and even the microstrip line design method.

Simulation and Test result

After the completion of the overall circuit design, the simulation is carried out. Because the circuit needs to work on the 2GHz operating frequency, the use of 2.5GHz clock to simulate the simulation. Simulation output SFDR waveform of 2.5GHz clock operation is shown in figure 8. From figure 8 it can be seen that the SFDR of the input signal amplitude of the circuit is about 64dB, of which the fundamental is 6.4dB, the second is 70dB.

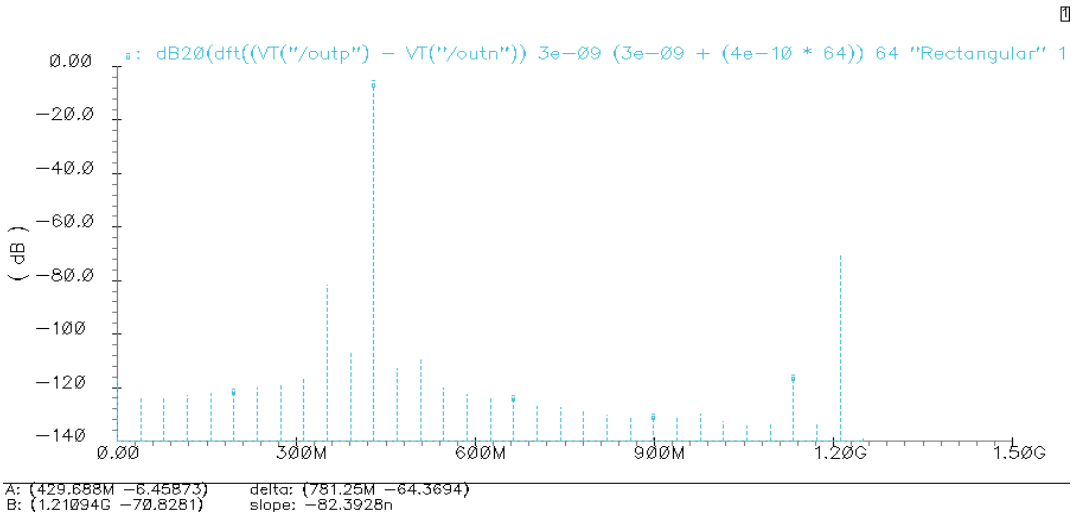
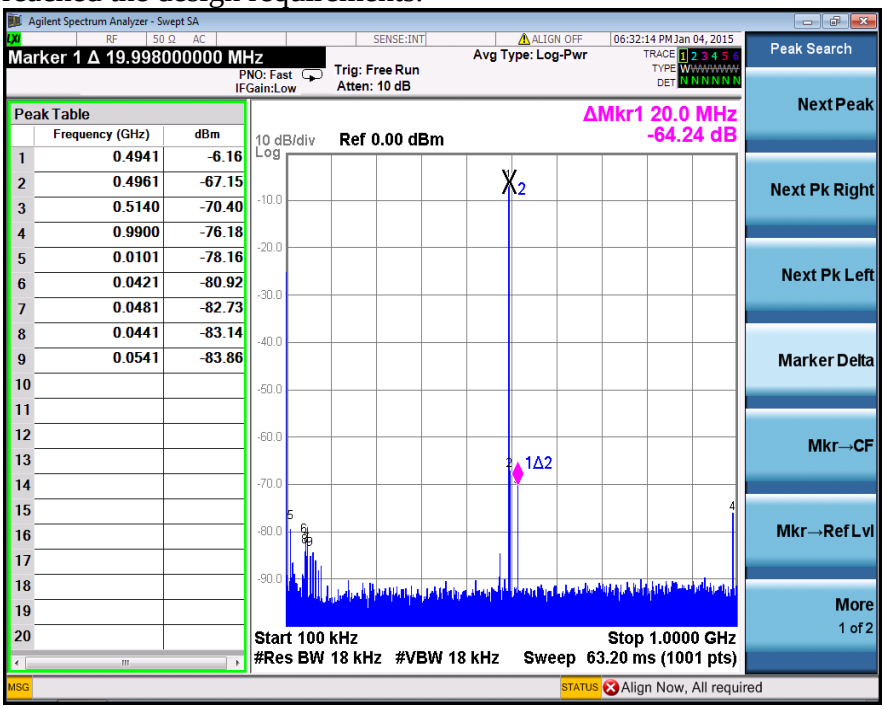
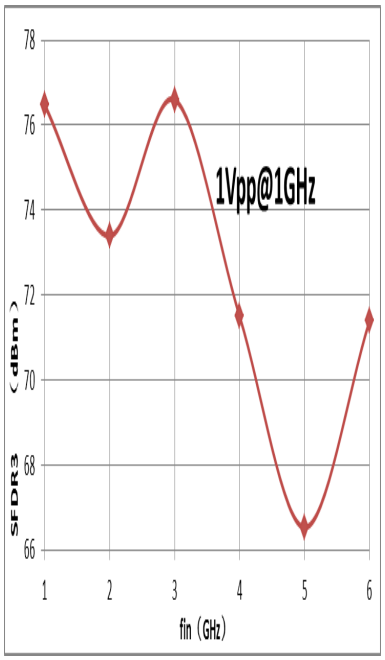


Fig.8. simulation output SFDR waveform

The actual chip in the SFDR 2GHz test waveform as shown in figure 9(a). As can be seen from Figure 9(a), the actual chip test results for the 2GHz clock sampling input signal 2.5GHz show that SFDR is 64dB,the fundamental wave is about 6dB, the second harmonic is 67dB, the SFDR3 is about 70dB. The test parameters are slightly worse than the simulation design values, but the basic reached the design requirements.



(a) test SFDR waveform @2GHz



(b)test curve of the SFDR3

Fig.9. the test results

From Figure 9(b) it can be seen that the track-and-hold circuit provides more than 66 dB hold-mode SFDR3 for 1.0 to 6.0 GHz.

Fig.10 shows the die photograph. The circuit is implemented in 0.18 μm HBT technology. The die area is 1.42mm×1.14mm.The power consumption of the chip is 570mW , when the positive power supply is 2V and the negative power supply is 3.3V.

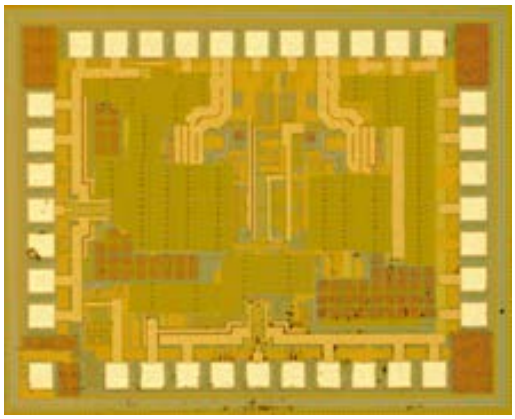


Fig.10. micrograph of the proposed track and hold circuit

The test results show that the main function of circuit is normal, preliminary implementation uses HBT device design of circuit target.

Conclusion

This paper presents a design of a 6GHz track-and hold circuit with input bandwidth. According to design of the core of track-and-hold circuit, input signal buffer circuit, output signal buffer circuit, sampling clock input circuit，the bias circuit and so on, Finally the track and hold circuit is designed, and has carried on the simulation and verification. The test results verified using HBT device to design the track and hold circuit initial success, the track and hold circuit can be used or integrated with a high-performance quantizer and a RF front end on a System-integration. The circuit is also exist certain optimization promotion space, will optimize the design in the following work.

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