An improved hybrid multilevel converter for renewable energy generation

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Abstract. This paper presents an improved hybrid multilevel converter for renewable energy generation. Topology and operating principles are investigated. Nearest Level Modulation (NLM) and control strategies under normal and dc fault conditions are studied. A 61 voltage-level model is set up in PSCAD/EMTDC. Simulation results validate the topology and its modulation and control strategies.

Introduction

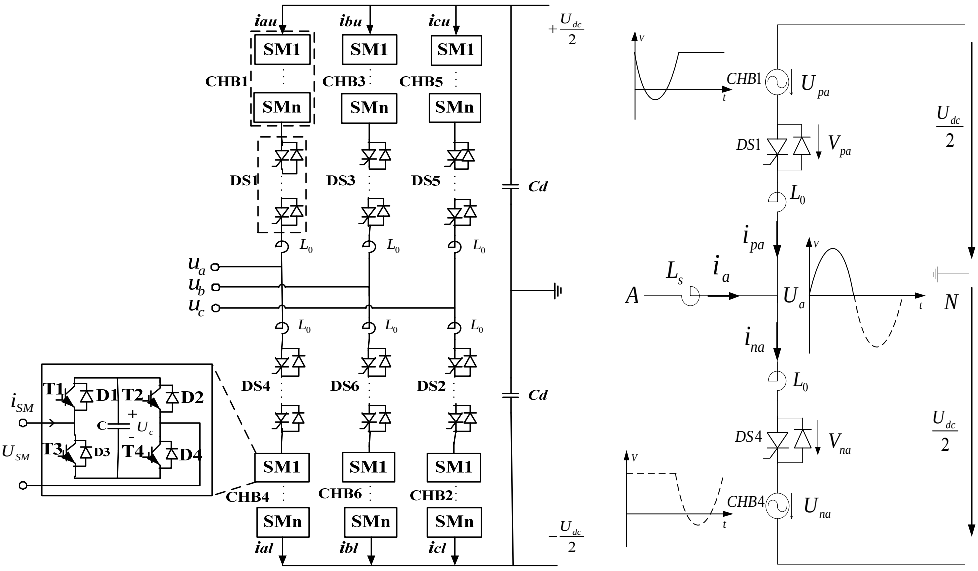
With the development of renewable energy (i.e. wind power and solar power) generation, its integration to the power grid has becoming a more and more important challenge. High voltage direct current (HVDC) transmission [1-2] is a suitable scheme for the integration. The key unit of HVDC is the converter. In general, there are two types of converters classified by the electronic devices. The one is named the current source converter (CSC) based on thyristors. The other one is named the voltage source converter (VSC) [3-4] based on insulated-gate bipolar transistors (IGBTs). The disadvantages of CSC are the probability of commutation failure, large harmonics, and inflexibility of power control. The advantages of CSC are high withstanding voltages and few losses. On the contrary, VSC has few harmonics and excellent output, but it has lower withstanding voltages and higher losses. And VSC cannot deal with direct current failure. To combine advantages of both topologies, an improved hybrid multilevel converter (HMC) is presented in this paper.

This paper is organized as follows. Topology and operation principles are introduced. And then control and modulation strategies are proposed. Verifications are made by PSCAD/EMTDC simulations.

Topology and Operating Principles

Topology

The structure of HMC, as shown in figure.1(a), has two essential parts: 1) cascaded H-bridges (CHB) composed of N series H-bridge sub-modules (SMs); 2) direction switches (DS), composed of series thyristors with anti-parallel diode. Each phase consists of two arms, conducting alternatively. Each arm is composed of a DS and a CHB. The SM has four states: 1) positively inserted; 2) negatively inserted; 3) bypassed; 4) blocked, corresponding to four output voltages: 1) Uc; 2) -Uc; 3) 0; 4) unknown (depending on the direction of the current through the SM).



(a) (b)

Figure.1 (a) Topology of the HMC; (b) Single phase equivalent circuit of the HMC

Operating Principles

When proper modulation method is adopted, CHB can be regard as a controllable voltage source. Taking phase A as an example, single phase equivalent circuit is illustrated in Fig.1 (b). As shown, the upper half cycle is generated by the CHB1 and the lower half cycle is generated by the CHB4. Assuming that the ac side is pure sinusoidal, the mathematic model is expressed as follow:

$$u_a(t) = U_m\cos(\omega t) \tag{1}$$

$$i_a(t) = I_m\cos(\omega t - \phi) \tag{2}$$

$$U_{pa} + G_{DS1}(t)u_a(t) = \frac{1}{2}U_{dc} \tag{3}$$

$$U_{na} - G_{DS4}(t)u_a(t) = \frac{1}{2}U_{dc} \tag{4}$$

$$G_{DS1} = \mathrm{sgn}(u_a(t)) \tag{5}$$

$$G_{DS4} = -\mathrm{sgn}(u_a(t)) \tag{6}$$

U_{pa} and U_{na} are the upper arm voltage and lower arm voltage respectively. Um and Im are amplitudes of ac voltage and current respectively. Function sgn(x) is the sign function.

Since thyristors are not self-closed device, the current change from the upper arm to the lower arm is as following principles. In order to ensure the thyristor closed, the phase relationship between ac voltage and current has to satisfy the relationship shown in Figure.2. When the voltage crosses zero from positive, the current must be positive. When the voltage crosses zero from negative, the current must be negative.

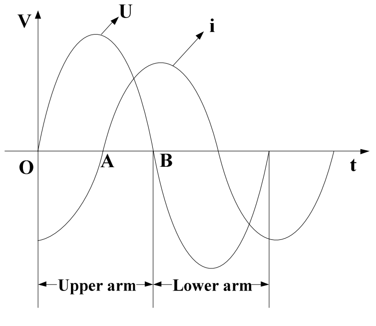


Figure.2 Phase relationship between voltage and current in HMC

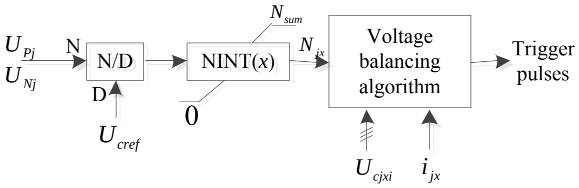


Figure.3 NLM strategy for the CHB

In order to ensure the energy balance between the ac side and dc side, there must be an ideal relationship between the ac side voltage and the dc side voltage. Following equations are used to derive the relationship.

$$\mathrm{P_{AC}} = 3\bar{\mathrm{U}}_\mathrm{a}\bar{\mathrm{I}}_\mathrm{a}\cos(\phi) \tag{7}$$

$$\mathrm{P_{DC}} = \mathrm{U_{dc}I_{DC}} = \frac{3}{\pi}\mathrm{U_{dc}}\hat{\mathrm{I}}_\mathrm{a}\cos(\phi) \tag{8}$$

$$\mathrm{I_{DC}} = \frac{3}{\pi}\mathrm{U_{dc}}\hat{\mathrm{I}}_\mathrm{a}\cos(\phi) \tag{9}$$

P_{AC} and P_{DC} are the ac side power and dc side power respectively. I_{DC} is the dc current. $\bar{U}_a$ and $\bar{I}$ are the RMS values of the ac voltage and current. $\hat{U}_a$ and $\hat{I}_a$ are amplitudes of the ac voltage and current. When P_{AC} is equal to P_{DC}, following equation is obtained.

$$\hat{\mathrm{U}}_\mathrm{a} = \frac{2}{\pi}\mathrm{U_{dc}} \tag{10}$$

Modulation and Control

Modulation method

Since the CHB has large number of H-bridges, the nearest level modulation (NLM) method is adopted [4]. Figrure.3 is the overall block diagram of the NLM modulation. To ensure the voltage balanced among all individual H-bridges, voltage balancing algorithm illustrated in Figure.4 is adopted.

Control strategy

Under normal condition, the active and reactive decouple control, shown in Figure.5, is adopted.

Taking the dc fault condition into account, HMC can change the control strategy to make the HMC work as a STATCOM.

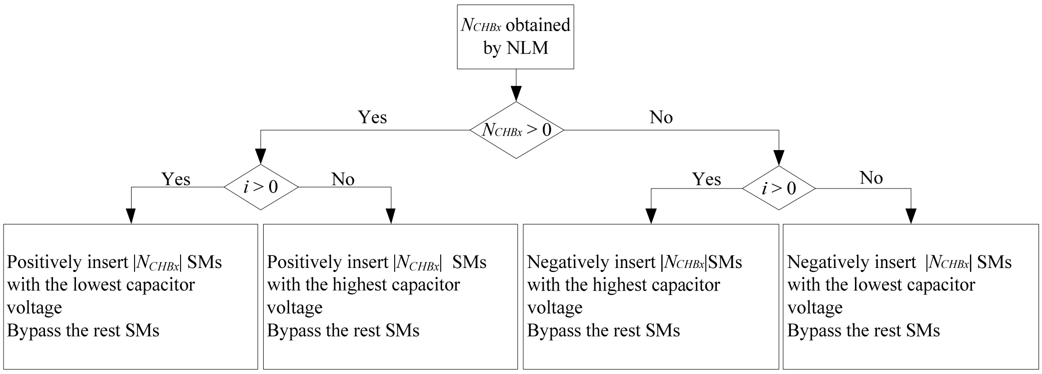


Figure.4 Voltage balancing algorithm

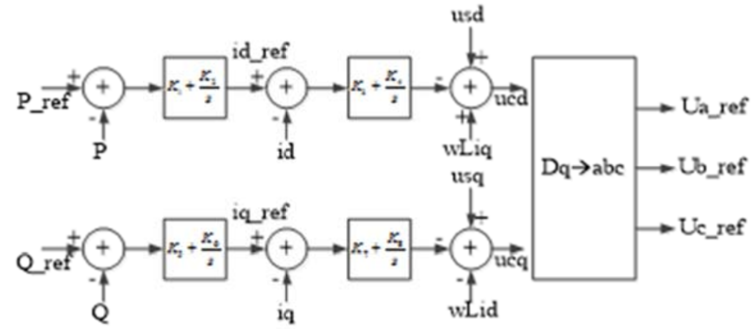
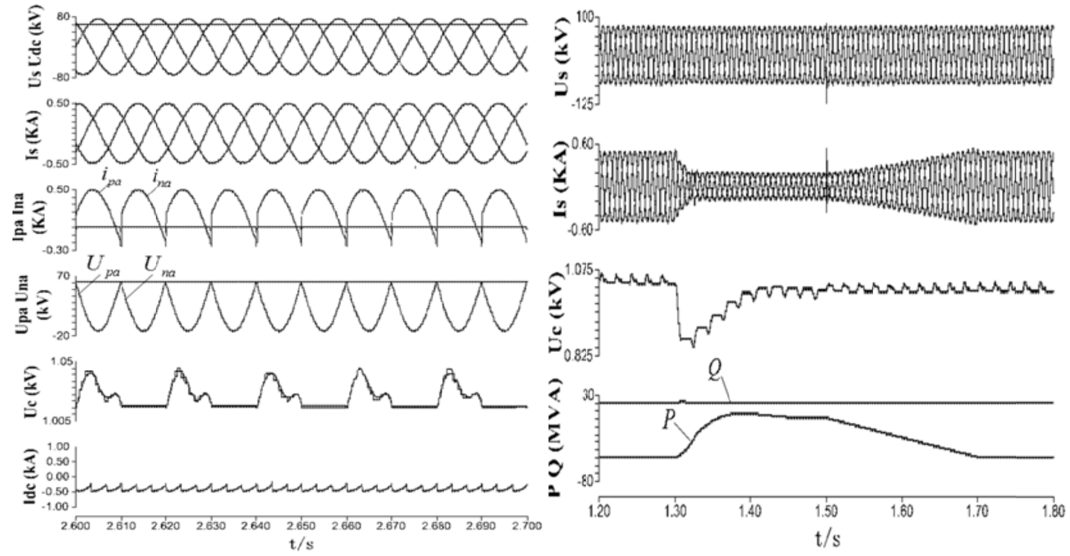


Figure.5 active and reactive power decouple control

Simulation Results

Parameters of simulation model are as follows: active power P is 50MW; reactive power Q is 20Mvar;ac voltage U_s is 90kV; direct voltage U_{dc} is 120kV; number of SMs in one arm is 60; capacitor voltage is 1kV.

Simulation results of normal condition and dc fault condition are illustrated in Figure.6 (a) and (b) respectively. The output performance is excellent during normal and dc fault condition.



(a) (b)

Figure.6 (a) normal condition (b) dc fault condition

Conclusions

In this paper, an improved hybrid multilevel converter used for HVDC is proposed. The topology and mathematic model are investigated. The modulation and control methods are presented. This proposed topology can ride-through the dc fault condition. Simulation results validate these strategies.

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