A design method for digital phase-locked loop

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Keywords: phase-locked loop; FPGA; digital processing; algorithm optimization ; coherent demodulation

Abstract.The design method of the digital phase-locked loop is presented，according to the parameters of the center frequency, the loop filter bandwidth, etc. The modules，phase detector(PD), loop filter(LF), voltage controlled oscillator(VCO)，have the similar behavior with that of the analog phase-locked loop(APLL) by using Laplace transform and bilinear transformation. For the case of lacking QuartusII license for numerical controlled oscillator(NCO) IP core, It can be replaced by the module designed by using triangle transform which is high-precision. Since enormous numbers of LEs in FPGA will be occupied by the multiplier of filters, the optimization algorithmis presented utilizingaddition operation and shifting operation rather than multiply operation, which reduces resources used on the system. The design result is simulated and realized on FPGA development board, which confirms that the design method is feasible.

Introduction

Phase-locked loop is widely used in the fields of electronics, communication, measurement and control, and automatic control. With the development of modern digital circuit technology, in the aspect of communication and control method of complex information processing can be implemented with the widely application of the microprocessor and VLSI. Phase-locked loop, as an important module in the communication fields, has the advantages of digital circuit in high reliability, low price, small volume and etc. Phase-locked loop is compatible with the digital circuit with better portability. Therefore, people pay more attention to the phase of the PLL, so that it is developed rapidly.

With the development of digital devices, digital phase-locked loop is applied to signal processing, modulation and demodulation, weak signal detection, frequency synthesis and so on. Compared with the traditional analog phase-locked loop, the digital phase-locked loop does not have the case of temperature drift. The design circuit is simply, meanwhile, filter parameters and the numerical control oscillator source are controlled by the code. It is easy to build a variety of high order loop PLL.

In this paper, according to the design example, design the parameters of the analog phase-locked loop. The digital processing of the analog parts is with the bilinear transformation. And use FPGA to simulate and implement it.

Basic theory of phase-locked loop

A typical phase-locked loop system is consist of three basic circuit components: Phase detector, loop filter and voltage controlled oscillator. As shown in Figure 1. Phase-detector detect phase deviation between input signal and feedback signal. Multiply the input signal with sinusoidal signal generated by a voltage controlled oscillator. Then the low pass filter is used to filter out the

radio-frequency component and get the phase difference between the input signal and the signal generated by the local oscillator. The phase difference is used as the control signal, controlling the voltage controlled oscillator by the correction network control network and using a negative feedback mechanism to reduce or eliminate the phase deviation of the input signal and the local oscillator signal.

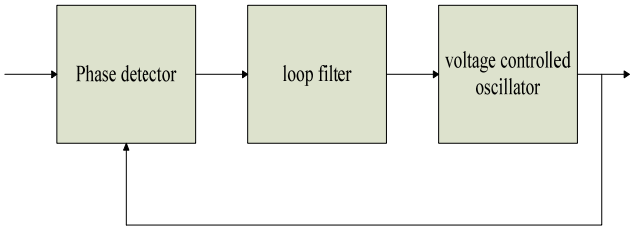

Fig 1.typical phase-locked loop

The digital phase-locked loop samples the analog input signal by the A/D into the FPGA. In FPGA, a phase detector, loop filter, and a numerical control oscillator module are built, making it to meet the same or similar operating performance of the analog filter.

Requirements of design examples

Designing an ideal two order loop digital phase-locked loop, carrier-frequency is $f_0 = 10kHz$, maximum modulating angular frequency is $\Omega_H = 103\,\pi\ \mathrm{rad/s}$, $K = 400 \times 2\,\pi\ \mathrm{rad/s}$, $\xi = 0.707$。

According to the design requirements, the natural resonance frequency is:

$$\omega_n = \frac{\Omega_H}{2.06} = 50\,\pi\ \mathrm{rad/s} \tag{1}$$

Tap parameters of loop filter:

$$\tau_1 = \frac{K}{\omega_n^2} \approx 0.10053 \tag{2}$$

$$\tau_2 = \frac{2\xi}{\omega_n} \approx 0.009 \tag{3}$$

According to the above parameters, the parameter values of the ideal two order ring loop filter simulator can be solved.

Digital processing of analog devices

The ideal two order loop can track the phase step signal and frequency step signal without error. Its transfer function can be expressed as:

$$F(s) = \frac{1+s\tau_2}{s\tau_1} \tag{4}$$

Because of the low pass characteristic of active proportional integral filter, therefore, the transformation of the S domain to the Z domain can be achieved by using bilinear transformation. According to the appropriate sampling period, the digital transformation of analog parts is realized.

$$s = c \cdot \frac{1-z^{-1}}{1+z^{-1}} \tag{5}$$

Substituting (5) into (4), getting the transformation from the analog domain F (s) to the digital domain F (z):

$$F(z) = \frac{\frac{1+c\tau_2}{c\tau_1} + \frac{1-c\tau_2}{c\tau_1} z^{-1}}{1-z^{-1}} \tag{6}$$

Converting (6) to time domain:

$$y(n) = y(n-1) + \frac{1+c\tau_2}{c\tau_1} x(n) + \frac{1-c\tau_2}{c\tau_1} x(n-1) \tag{7}$$

Simultaneously taking the coefficient $c = \frac{2}{T} = 2f_s{}' = 100kHz$, and it can be obtained $c\tau_1 = 10053$, $c\tau_2 = 900$. The time domain expression of the digital processing of the analog phase locked loop filter is obtained:

$$y(n) = y(n-1) + \frac{901}{10053}x(n) + \frac{899}{10053}x(n-1) \quad (8)$$

Designing the low pass filter for phase detector，the passband frequency is 1kHz, the cutoff frequency is 10kHz. Low complexity and digital low pass filter is designed by MULTISIM tool. It is obtained by the two identical RC filtering networks. The simulation parameters are R=1kΩ，C=0.1μF.

Transfer function for low pass filter:

$$H(s) = H_1(s) \cdot H_2(s) \quad (9)$$

In type (9)，$H_1(s) = H_2(s) = \frac{1}{1+s\tau}$, $\tau = RC = 10^{-4}$. Using digital processing of transfer function $H_1(s)$and through bilinear transformation, we get:

$$H_1(z) = \frac{\frac{1}{1+c\tau}(1+z^{-1})}{1+\frac{1-c\tau}{1+c\tau}\cdot z^{-1}} \quad (10)$$

In type (10)，$c = \frac{2}{T} = 1\text{MHz}, c\tau = 200$.Time

domain:

$$y_1(n) = \frac{199}{201} \cdot y_1(n-1) + \frac{1}{201} \cdot [x(n) + x(n-1)] \quad (11)$$

By the type (11), the IIR filter is obtained. IIR filter can be implemented by multiplier and divider in FPGA. These two devices need to consume a large amount of LE resources of FPGA. Using specific sampling frequency can convert the multiplication and division into shift and addition and subtraction. That can save a lot of system resources.

For shaping as a digital time domain formula:

$$y(n) = \frac{a-1}{a+1} \cdot y(n-1) + \frac{1}{a+1} \cdot [x(n) + x(n-1)] \quad (12)$$

Selecting the appropriate “a” to make a+1=2^N, which N is an integer.

The above type can be written as:

$$2^N \cdot y(n) = 2^N \cdot y(n-1) + x(n) + x(n-1) - 2 \cdot y(n-1) \quad (13)$$

When $c = \frac{2}{T} = 1.275\text{MHz}, c\tau = a = 255$

Getting：

$$2^8 \cdot y(n) = 2^8 \cdot y(n-1) + x(n)x(n-1) - 2 \cdot y(n-1) \quad (14)$$

According to the type (14), IIR filter from the multiplication and division operation converts into shift and addition and subtraction operation. That saves a lot of system resources.

Then, low pass filter module is cascaded to obtain a low pass filter which meets the requirements in FPGA.

Parameter design of FPGA module FPGA

Voltage controlled oscillator of analog PLL becomes numerical control oscillator when be digitized. We can use its own numerical control oscillator IP core in Quartus II. FPGA's system clock is 80MHz. The sinusoidal signal generated by the free oscillation frequency is 10KHz. Using 32 points sampling, then the average of each phase takes 250 system clock period. If K=400Hz，then the value range of NCO is [-10,10].Because of large adjustable frequency interval of NCO causes the instability of the loop. Adjustable frequency interval of NCO should be reduced. The design uses the center frequency ω_0 and the controllable frequency offset frequency Δω. Namely, the frequency with $\omega_0 + \Delta\omega$ of sinusoidal signal can be produced by the following way:

$$cos[(\omega_0 + \Delta\omega)\, t] = cos(\omega_0 \cdot t) \cdot cos(\Delta\omega \cdot t) - sin(\omega_0 \cdot t) \cdot sin(\Delta\omega \cdot t) \quad (15)$$

In type，$\omega_0 = 20000\pi\text{rad/s}, -800\pi < \Delta\omega < 800\pi$.Figure 2 is structure diagram of NCO, The stable output of each frequency point can be obtained by the accurate control of the offset frequency.

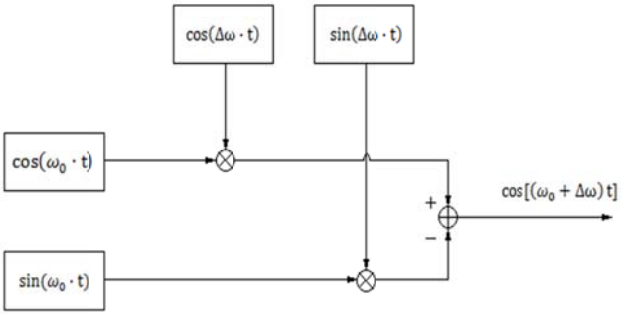

Fig 2.NCO design scheme in FPGA

Sine wave output data is 8bit signed data, range of values is [-127,127]. After mixing the output range is [-16129,16129], The data changed into a low pass filter is [-8064,8064]. The AC gain of the loop filter is $\frac{\tau_2}{\tau_1} = \frac{900}{10053}$, then the output range of the loop filter is [-722,722]. Conducting linear adjustment of the output of the loop filter so that it is mapped to the NCO input.

System testing and verification

The design uses cyclone IV ALTERA series FPGA chip to achieve. Design software to develop is the QuartusII 11 of the company. Inputting10.050kHz signal, the deviation of the center frequency is 50Hz. Using Signal-Tap intercept test state. Figure 3 is the synthesis results of the digital phase locked loop which is prepared by above method.

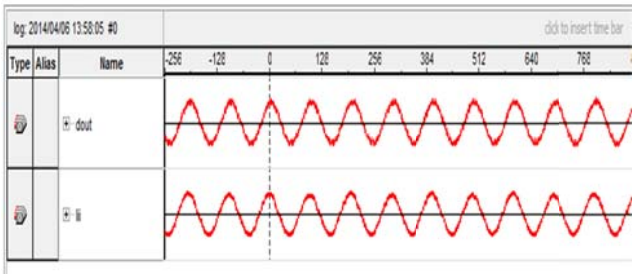

Fig 3.test results of digital phase-locked loop

Li is the input of the carrier signal and dout is tracking output signal of NCO in figure 3. clearly seen from the picture, NCO tracking output can be very good to lock the phase and frequency of the input signal.

Conclusion

In this paper, design parameters of analog phase-locked loop according to design requirements. Using the bilinear transformation get the transformation of the s domain to the Z domain. This design uses Verilog programming language. It is implemented by the cycloneIV series FPGA chip of ALTERA. And verification by Signal-Tap tool, the results show that the system can meet the requirements. Analog phase-locked loop becomes digital processing in FPGA. It has the advantages of good portability, small size, high reliability, convenient maintenance and upgrade, etc., and enhance the reliability and stability of the system.

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