Fabrication and Characterization of 1200V 40A 4H-SiC SBD

Gang Chen[1, 2, a], Yinglu Fang[2], Yun Li[1], Lin Wang[2], Song Bai[1, 2], Ao Liu[2], Runhua Huang[2], Yonghong Tao[2], Zhifei Zhao[1]

[1] State Key laboratory of Wide-bandgap Semiconductor Power Electronics, Nanjing, China

[2] Nanjing Electronic Devices Institute, Nanjing, China

[a] E-mail: steelchg@163.com

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Abstract: High voltage 4H-SiC Ti schottky junction barrier schottky (JBS) diode with breakdown voltage of 1200 V and forward current of 40 A has been fabricated. A low reverse leakage current below 1.02×10^{-4} A or 4.08×10^{-4} A/cm^2 at the 25 ℃ and the reverse bias voltage of 1200 V has been obtained. The forward on-state current was 40 A at $V_F = 1.61$ V with 25℃ and at $V_F = 1.89$ V with 100℃. The chip is 5 mm × 5 mm and the active-region is 3.8 mm × 3.8 mm. The turn-on voltage is about 0.83 V. The on-state resistance is 4 mΩ·cm^2. The doping and thickness of the N-type drift layer and the device structure have been performed by numerical simulations. The SiC JBS devices have been fabricated and the processes were in detail. By using Ti/Ni/Au multilayer metal structure, the double side Au process of 4H-SiC JBS diode is formed.

1. Introduction

The power devices are mainly fabricated using silicon as the semiconductor material. Si device design and fabrication technology has matured over the past six decades. 4H-SiC has been shown to have tremendous potential for high power electronic devices.[1] SiC power devices has been a stable segment in the power electronics market in recent years. We have already reported a high-voltage (>2 kV) Ti/4H-SiC SBD fabricated on 12 um thick 4H-SiC epilayer with B+ implantation edge termination and field plate technology.[2]

In this article, we report our progress research on epitaxial thickness, doping and DC and experimental results of 1200V 40A 4H-SiC SBD. The fabrication process is also described in detail.

2. Design and Experimental

High-voltage 1200V 40A 4H-SiC diodes have been fabricated in a newly developed processing sequence, using standard silicon process equipment. Epitaxial layers grown by chemical vapor deposition (CVD) on commercial 4H-SiC substrates were used as starting material for implanted p+-n−-n+ merged pn-Schottky (MPS) diodes, together with additional test structures. [3] The epitaxial structure view and thickness map of a 4H-SiC epitaxial wafer of 1200V 40A SBD are shown in Fig. 1. The average thickness of 4H-SiC epitaxial layer is 11.6um, the minimum value is 11.1 and the maximu value is 12.2um. A successful design of the SiC SBD is shown in Fig. 2. The SiC SBDs are fabricated on a highly doped n+ 4° off-axis Si-face 4 inch 4H-SiC substrate with epitaxially grown n^+ buffer, n^- drift layers. The Schottky contact layer is 11.6μm thick and doped to $n^- = 6.5 \times 10^{15}$ cm^{-3} for Ti / SiC Schottky contact formation. The n^+ buffer layer is 1μm thick and doped to 1×10^{18} cm^{-3}. The n^- type drift layer is designed to block over 1200 V. Both Schottky and PN diodes were processed on the same wafer to fabricate Schottky contacts on n-type epilayer and ohmic contacts on implanted p-type regions, respectively.[5] Optimize the device's structure design through a finite element analysis and adopt 10 terminal protection guard rings according to the results. The width of the Schottky contact surface in active region is 5um and the width of implanted P^+ region is 1um. The width of 10 terminal protection guard rings is 3um and all the rings are in the 70um width region. The terminal protection guard rings are formed with Al^+ implanted simultaneously with the P^+ region of the active region. An activation annealing was carried out at 1850℃ for 3 min in Ar ambient. The n^-

Schottky regions and p^+ regions are simultaneously metallized with Ti with the e-beam evaporation and annealed at 450 ℃.[4] Excluding the bonding pads and edge termination regions, the single chip has a total area of 25 mm^2 (5 × 5 mm^2). The back side Ni ohmic metal layers are annealed at 900 ℃ with n^+ 4H-SiC to form nickel silicide ohmic contacts. By using Ti/Ni/Au multilayer metal structure, the double side Au process of 4H-SiC JBS diode is formed.

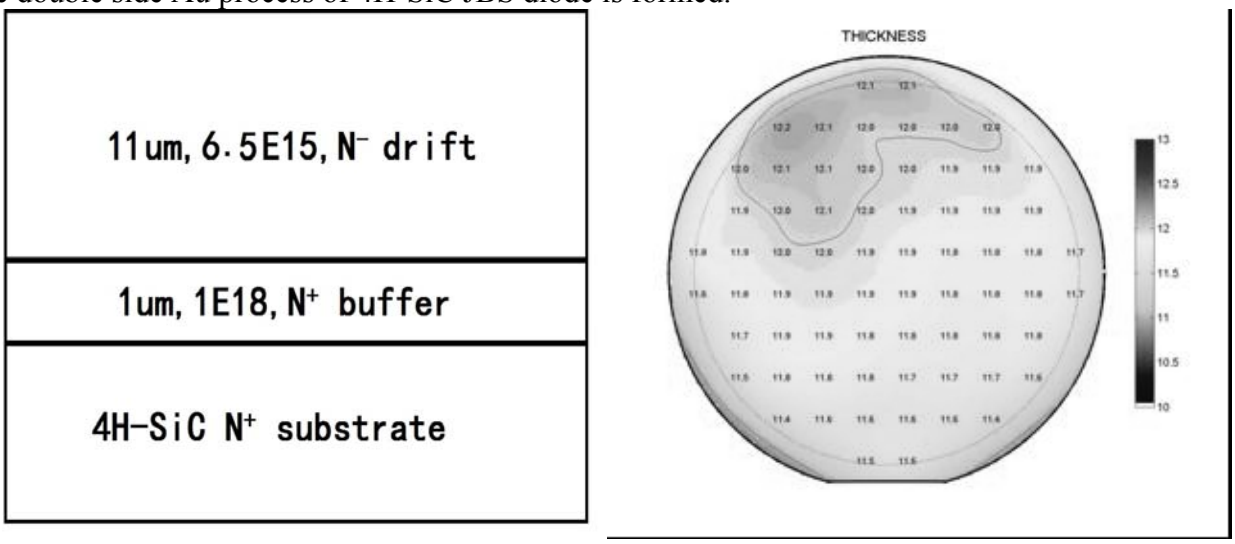

Fig. 1 Cross sectional view and thickness map of a 4H-SiC epitaxial wafer for 1200V 40A SBDs

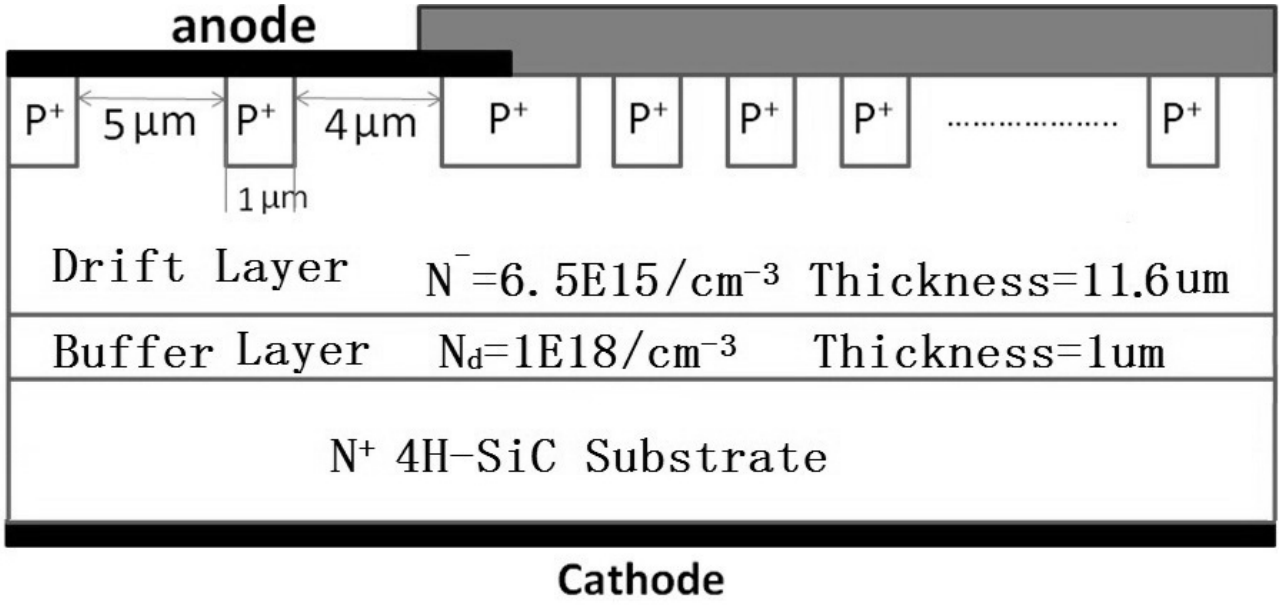

Fig. 2 A designed image of the 1200V 40 A SiC SBD

3. Results and discussions

Tektronix 370 is used to measure the devices. From Fig. 3, we can know that the 1200 V 40 A SiC SBD device yielded a forward current 40 A at a forward voltage of 1.61 V at 25 ℃, 1.67 V at 50 ℃, 1.79 V at 75 ℃, 1.90 V at 100 ℃. The device has a specific on-resistance of 4 mΩ·cm^2 at 25 ℃, 4.6 mΩ·cm^2 at 50 ℃, 5.35 mΩ·cm^2 at 75 ℃, 6.1 mΩ·cm^2 at 100 ℃, considering the guarding rings area. From Fig. 4, we can know that, at the forward voltage of 1.5 V, the 1200 V 40 A SiC SBD device yielded a forward current 34 A at 25 ℃, 31 A at 50 ℃, 26 A at 75 ℃, 24 A at 100 ℃. During the temperture increased from 25 ℃ to 100 ℃, the degradation of the forward current is 30 % , the degradation of the forward voltage is 18 %, the degradation of the specific on-resistance is 52.5 %. The 1200 V 40 A SiC SBD devices are viable high temperature alternatives. As illustrated in Fig. 5, the room temperature 1200 V 40A SiC SBD device's blocking voltage is 1200V at reverse leakage

current equal to 102 μA. More comprehensive test data taken at higher temperatures will be presented later.

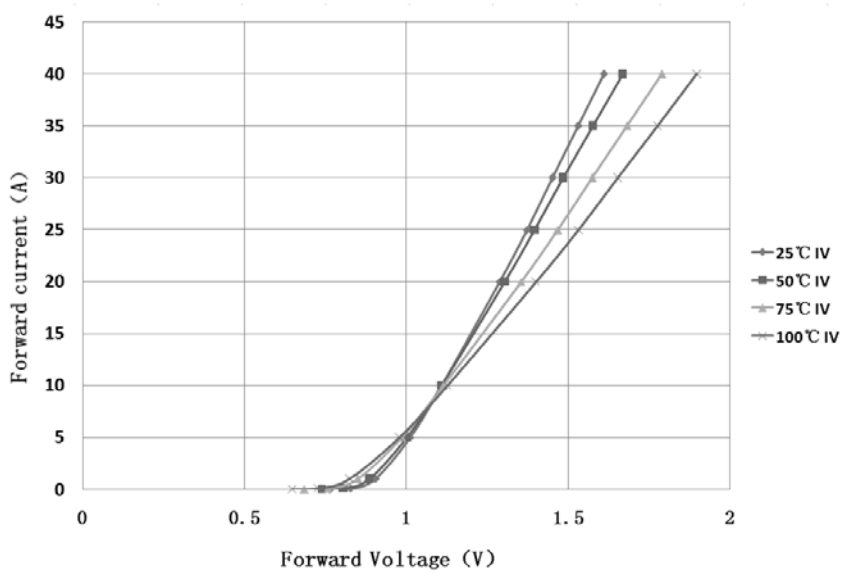

Fig. 3 Forward I-V characteristics up to 40 A with V < 2 V for 1200 V 40 A SiC SBD, temperature from 25 ℃ to 100℃.

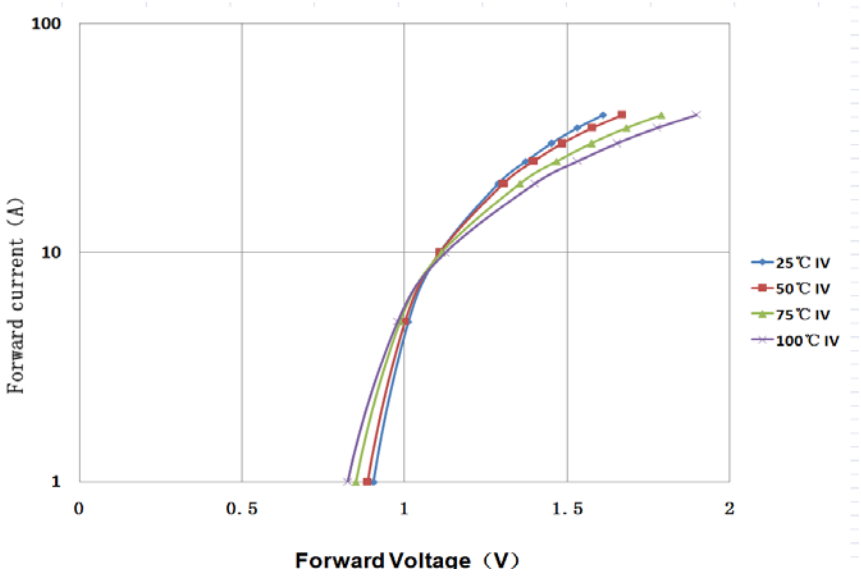

Fig. 4 Logarithmic scale forward I-V characteristics 1200 V 40 A SiC SBD

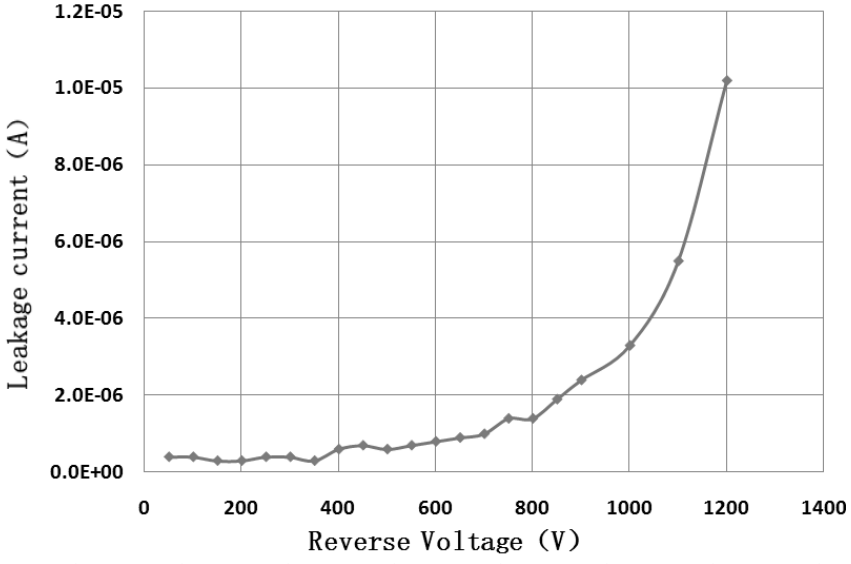

Fig. 5 Reverse I-V characteristics 1200 V 40 A SiC SBD

4. Conclusions

1200 V 40 A SiC SBD devices on n+ conductive 4H-SiC substrates have been fabricated. The double side Au processes and the package of the SiC JBS were developed and high performance of the SiC JBS device was reported. By employing a high energy ion implantation and high temperature annealing technique, excellent characteristics were obtained. The breakdown voltage can be improved to more than 1.2 kV depending on device guard ring termination structure. A low reverse leakage current below 4.08×10^{-4} A/cm^2 at the bias voltage of -1.2 kV has been obtained. The forward on-state current was 40 A at $V_F = 1.61$ V at 25 °C and 160 A/cm^2. The fabricated diodes can be used in high temperture, high-voltage, high-current switching test systems.

Next step is to optimize the fabrication in order to get a lower reverse leakage and higher forward conduction. Further work will focus on more extensive studies of the reverse recovery waveforms and reverse capability of the fabricated JBS diodes at higher temperature.

Acknowledgments

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