Real-time Mechanical Parking Equipment Image Acquisition and Preprocessing Based on FPGA

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***Abstract*—As mechanical parking equipment are developing to be complicated, intelligent and familial oriented. The real-time image acquisition and preprocessing of mechanical parking equipment based on CMOS camera and FPGA were proposed to improve the intelligent level and decrease the number of service personnel. The system is constituted by five parts ,i.e., SCCB bus control module, image capture module, image storage module, image preprocessing module and VGA display control module. Using FPGA Cyclone II family chips as the core controller, The CMOS OV7670 image sensor initialization module, image acquisition and storage module, VGA interface protocols, VGA horizontal synchronization and field sync signal were designed using Verilog HDL. The grayscale processing and the fast median filtering algorithm were adopted to preprocess mechanical parking equipment image in FPGA. The experiment results shows that the image after preprocessing can real-time displayed by VGA, and also the system based on FPGA can design flexibility, portability strong, and it can achieve high-speed acquisition and high compatibility.**

Keywords—FPGA; Image acquisition; VGA display; Image processing

I. INTRODUCTION

Complicated, intelligent and highly automated are the mechanical parking equipment developing directions, Image processing technology in mechanical parking equipment mainly embodied in the following three aspects. First, in large warehouse-style flat mobile class stereo garage, rotary robots and lefts can move the car to the assigned parking spaces through image acquisition and recognition , which can avoid traffic conflict of car inbound and outbound effectively. Secondly, the application of image recognition technology, navigation, positioning technology and sensor technology to the garage, the driver can real-time monitor the dynamic information of vehicle storage by phone , Real-time tracking the storage location of the car, find the assigned parking information through mobile phone positioning guide[1] .Thirdly, developing automatic license plate recognition system using image recognition for mechanical parking equipment intelligent parking management system, which can identify the illegal information from license plate number, and to dynamic tracking of illegal vehicles, At the same time, it can greatly shorten the waiting time in the garage parking workspace ,thereby greatly improving the working efficiency of the garage [2]。

Traditional image acquisition and processing technology is a computer terminal receives the image information acquired by card collection, because of its long development cycle, bulky, hard to expand [3], it is difficult to meet the needs of modern intelligent mechanical parking equipment. It is analyzed the advantages and disadvantages of DSP or FPGA in image processing in literature [4], and point out that the FPGA has the characteristics of hardware implementation and parallel processing, so PFGA have a greater advantages than the DSP in the image data processing[4]. CMOS image sensor with low power consumption, high integration and easy design to a single chip system, and has a greater affinity with FPGA, so the combination of FPGA and CMOS can speed up development [5], and can guarantee higher data bandwidth in video capture system [6].

In this paper, a mechanical parking equipment image acquisition and preprocessing system based on FPGA and CMOS image sensor is presented. The structure of the system, image acquisition, image storage, image preprocessing, image display and other aspects have studied in this paper. The CMOS OV7670 sensor was controlled by SCCB, the Samsung K4S641632K model SDRAM memory was used to cache the image data, the digital image signal and VGA analog signal's conversion were complete by the ADV7123 analog-to-digital conversion chip. In order to reduce the amount of subsequent image processing data, gray-scale transforming and median filter processing, completed by FPGA image preprocessing, which can reduce noise, and further improve real-time systems..

II. SYSTEM ARCHITECTURE DESIGN

The hardware part of this system is composed of OV7670 CMOS camera module, FPGA core controller, SDRAM memory and ADV7123 analog-to-digital conversion chip, as show in Figure1. Software system consists of image acquisition, preprocessing, storage, and image display and so on. The Altera's Cyclone II EP2C35F484C8N chip acts as the master chip, the SCCB sequence for OV7670 control generated by FPGA internal I2C control module. In Streaming data capture module, the 8 bits image data captured by OV7670 are converting to 16 bits YCrCb image information, which will transmitted to video data preprocessing module. The underlying image processing, such as the image grayscale

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processing, median filtering, edge detecting and so on , are completed in video data pre-processing module. Horizontal sync and vertical sync signals for ADV7123 generates by VGA timing module, the processed image data are displayed on screen through ADV7123 analog-to-digital conversion chip.

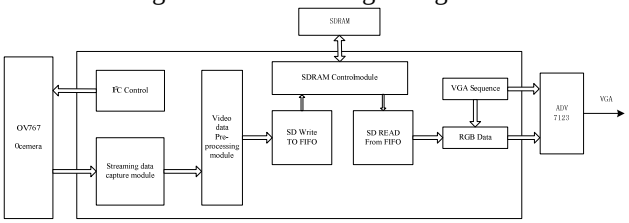


Figure (1) System structure diagram

III. OV7670 VIDEO CAPTURE MODULE DESIGN

When image capturing, the OV7670 image sensor need to meet two conditions,(1) video streaming valid only in Pclk rise state, (2)it is need 10 frame delay for the register modification. The flow chart of video image capture as shown in Figure (2).

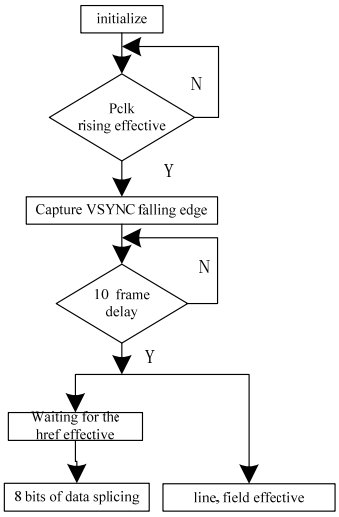


Figure (2) The flow chart of video image capture

IV. MEMORY MODULE DESIGN

This system adopts capacity of 4 MB x 16 K4S641632K SDRAM produced by Samsung Company. Each bank of this SDRAM consists of 2018 lines and 256 columns of 16 storage array, the maximum storage frequency is 166MHz. SDRAM must be constantly updated to keep data, each update command can only work in a row, so, it's must be complete one times update command within 64ms/2048=15.625us intervals, periodically refresh to keep data in SDRAM. Figure (4) shows the memory structure.

SDRAM controller is mainly composed of initialization and configuration module, control interface module, clock module, data reading and writing FIFO module and command parsing module, as shown in figure (3)[7]. Initialization and configuration module mainly complete the control of FIFO reading module and FIFO writing module and SDRAM initialization, after power on the SDRAM in this system, which enters a stable period for 200us, then pre-charging for 0.2us, then do 8 cycles automatic update, then after mode setting for 0.2us, then will enter normal read and write and update, Finally, it will enter the normal read, write and update operations. And Producing write SDRAM request signal, and read SDRAM request signal.

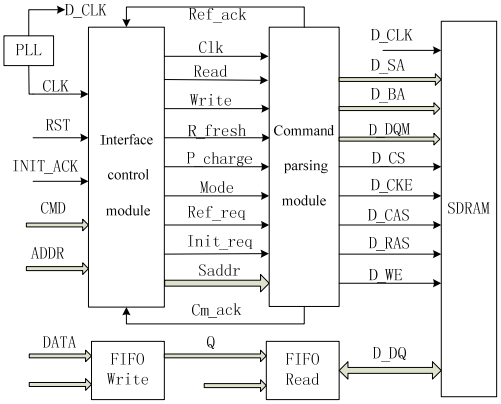


Figure (3) The memory control chart

Interface control module is mainly to realize the interface instructions initialization and generate decoded instructions, the 'NOP', 'READ', 'WRITE', 'R_fresh', 'P_change', 'Mode ' instruction are decoded in the interface control module and then transferred to the command parsing module, The 'R_fresh' instruction in interface control module is mainly composed of a down counter and the corresponding control circuit，and generates a refresh request command for the command parsing module, when the down counter output is 0, the interface control module immediately send refresh request 'Ref_req' to command parsing module, and keep the 'Ref_req' signal valid .

V. VGA DISPLAY CONTROL MODULE N

The acquisition image signal will be showed in VGA display, when it is operated by the color space conversion and median filtering processing. VGA display requires 0~0.714V analog signal, In order to realize the interface matching between FPGA and VGA, a DAC analog conversion circuit need to be designed to solve the 0~0.714V analog video signal output. A professional video conversion ADC chip ADV7123 was used to solve the problem. The circuit schematic diagram of the ADV7123 is shown in Figure (4).

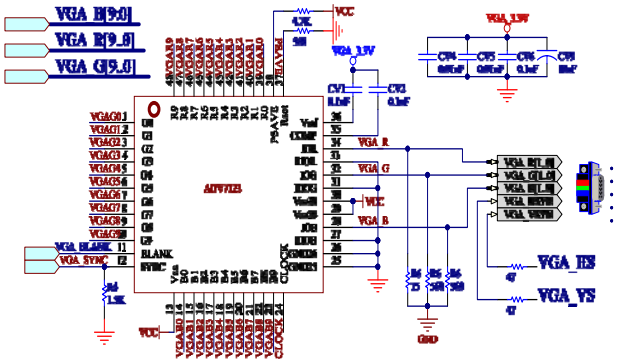


Figure 4 The circuit schematic diagram of the ADV7123

The system hardware is composed of timing signal module, image storage module and user selection module, as shown in Figure (5). FPGA as the main controller to control the whole system. This article uses the VGA resolution of 640 x480 industrial standard [8]. Figure (6) shows HuZhou vocational and technical college of Chinese characters thought VGA display.

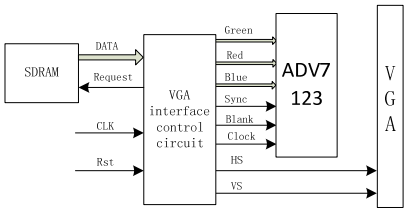


Figure (5) system hardware block diagram

Figure (6) VGA display Chinese characters

VI. IMAGE PREPROCESSING MODULE DESIGN

A. Color space conversion module

Generally,real-time image processing always carry out in the gray image state,for example, Image filtering, Sobel algorithm, image recognition technology and so on . so it's need to convert RGB color space to the YCrCb color space. The calculation method to convert image from RGB color space to the YCrCb color space, as shown in equation (1)[9].

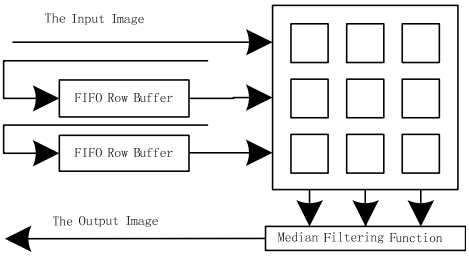
$$\begin{bmatrix} Y \\ C_r \\ C_b \end{bmatrix} = \begin{bmatrix} 0.299 & 0.578 & 0.114 \\ 0.500 & -0.4187 & -0.0813 \\ -0.1687 & -0.3313 & 0.500 \end{bmatrix} * \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix} \quad (1)$$

Verilog HDL language can not be calculated on the float, so the equation (1) expanding 256 times and then moves to the right way of eight bits to complete hardware language preparation. equation (2) are the formula after conversion.

$$\begin{bmatrix} Y \\ C_r \\ C_b \end{bmatrix} = \left\{ \begin{bmatrix} 77 & 150 & 29 \\ 128 & -107 & -21 \\ -43 & -85 & 128 \end{bmatrix} * \begin{bmatrix} R \\ G \\ B \end{bmatrix} >> 8 \right\} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix} \quad (2)$$

B. Fast median filtering module

Noise is generated in the car image acquisition, decoding, reading and writing process and so on, which reduce the quality of the image,so fast median filtering algorithm is used to eleminate noise interference, the median filtering module consisted of by two FIFO module and 3x3windows , Algorithm block diagram as shown in figure (7)[10].



Figure（7）Fast median filtering module

VII. ANALYSIS

The Verilog HDL language is used to complete the system hardware circuit design, the synthesis,analysis and implementation are carried on in Quartus II design software, the chip resource utilization as shown in Table (1)

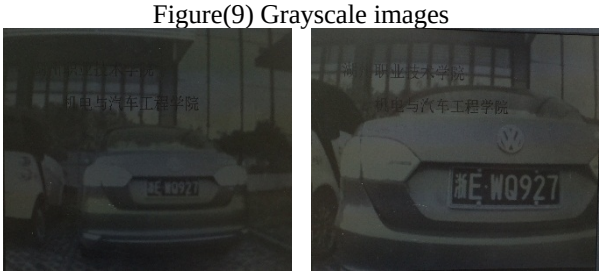
Table (1) FPGA resource utilization

resource	Use Number	Number Available	usage rate (%)
Logic elements	1226	33216	4
combinational functions	1099	33216	3
dedicated logic registers	536	33216	2
pins	96	322	30
memory bits	40960	483840	8
multiplier elements	0	70	0
plls	1	4	25%

The original color images captured by CMOS OV7670 camera are shown in Figure (8), the grayscale images obtained by real-time color space conversion in FPGA are shown in Figure (9), the images obtained by fast median filtering are shown in Figure (10). By comparing Figure (9) and (10) found that the grayscale images shown in Figure (9) have some noise, and after a fast median filtering processing in Figure (10) can effectively filter out the noise around the image.The image in Figure(10) can be processed by upper algorithm for further processing.

Figure(8) Original image

Figure(9) Grayscale images



Figure(10) Fast median filter image

VIII. CONCLUSION AND SUMMARY

Aimed at the development direction of intelligent mechanical parking equipment,The image acquisition and pre-processing systems based on FPGA and CMOS image sensors was designed for mechanical parking equipment. Research on system structure, image acquisition, image storage, image pre-processing, image display, etc., the images which processed by fast median filtering algorithm can achieve a rapid de-noising image, and can be displayed in VGA. The system has a short development cycle, low cost, high flexibility characteristics. Thus, the system has not been used on mechanical parking equipment, the next step is to develop control system based on machine vision

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