A Design of Passband-chosen Complex Filter and Automatic Calibration System

Xi Zeng[1, a], Weidong Geng[1, b*] Yunqian Zhang[1, c] and Wenshen Wang[2, d]

[1]Institute of Photo-electronics Thin Film Devices and Technique of Nankai University ,
Key Laboratory of Photo-Electronics Thin Film Devices and Technique of Tianjin ,
Key Laboratory of Opto-electronic Information Science and Technology, Nankai University,Tianjin 300071, China;

[2] Beijing Langboxinwei Electricon Company, Beijing 100084, China.

[a]zengxi1213@126.com, [b]gengwd@nankai.edu.cn, [c]zhangyq_nku@163.com, [d]wenshen.wang@rfmc.com.cn

*Corresponding author: Weidong Geng: gengwd@nankai.edu.cn

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Abstract. A low power design of active RC complex filter was proposed by using 130nm CMOS process. The filter has 4 center frequencies, 100 kHz, 200 kHz, 300 kHz and 500 kHz. The image rejection is higher than 40dB. An automatic calibration system with dichotomy algorithm and RC oscillator circuit was used to caliber both the center frequency and the band-wide. The circuit consumption of the filter and the calibration system is less than 500uA with 1.5Vsupply voltage and the calibration error is less than 1%.

1. Introduction

Low-IF wireless communication receiver has attracted great attention of recent research and development with the advantage of avoiding DC offset. However, the signals from the mixer of the low-IF receiver has been mixed with mirror signals [1], which are different to be distinguished with the normal signals, resulting in a great interference. The popular solution to reject the mirror signals is to use a complex filter [2]. Besides, most wireless communication devices work with internal battery-powered, so low power design of complex filters becomes a hot research spot. In reference [3], a 3-orders active RC complex filter with an integrator and a digital circuit has a bandwidth of 20MHz, a center frequency of 46 MHz, and its current consumption is less than 7.9mA with the power supply of 1.8V. In reference [4], a 12-orders complex filter with controllable transconductance has bandwidths of 0.5~1.5MHz and 1~3MHz, center frequency of 1MHz and 2MHz and its power consumption is 2.77mW. Reference [5] shows a 3-orders RC complex filter applying for ZigBee, whose bandwidth is 3.09MHz, center frequency is 2MHz and current supply is 1.2mA with the working voltage of 1.8V. Traditional complex filters provide only one passband or two passbands, resulting in the application of the chips limited. Based on the SMIC130nm, this paper has proposed a 4-passbands complex filter applying for RFID, shown a capacitor array with miller compensation in order to keep the stability of the circuit and given a RC calibration module to solve the craft error.

2. Design of Complex Filter

2.1 Circuit of Complex Filter

The active RC filter has a lower noise, large output range and better stability [6] [7], which was used in this paper. For multi-stage complex filter, how integrators make multi-stage filter influences its dynamic range and the accuracy, among which filter made of the leapfrog structure has a smaller parasitic sensitivity and bigger dynamic range [8], chosen by the Butterworth filter in this paper. Besides, the more the order of the filter is, the higher its image rejection is and the more the power consumption is, in certain center frequency and bandwidth. In order to achieve the request of the

image rejection of 40dB, the complex filter in this paper uses 3-order leapfrog Butterworth structure for I/Q signal channel. The circuit of the complex filter shown as Fig.1, which is made of two identical 3-order leapfrog Butterworth LPF with 4 bandwidth, 60 kHz, 120 kHz, 200 kHz and 275 kHz. Under the role of the frequency resistors R_{if}, connected between I channel and Q channel, the center frequency is changed from 0 to the target center frequency [9].

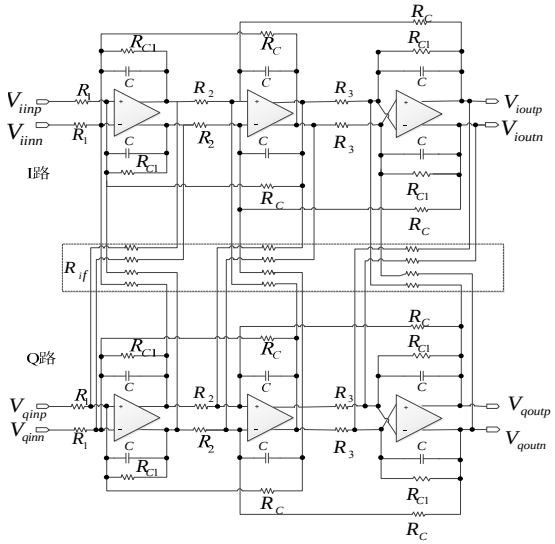

Fig.1 3-order leapfrog complex filter

2.2 Design of Amplifier

Amplifier is the key unit of the active RC filter, whose performance, especially the GBW [10], determines the capability of the filter directly. The GBW must be 50~100 times of its cutoff frequency from experience. The most bandwidth of the filter proposed in this paper is 275 kHz, so the least GBW of the amplifier used in the circuit is 13.75MHz. In order to obtain high gain and high load drive capability in the case of small layout area and power consumption, two-stage amplification structure is used in this paper. From the simulation result shown as Fig.2, it is seen that the GBW of the amplifier is 32MHz, PM is 69.24° and DC gain reaches 72dB, satisfy the requirement of the filter.

The ac simulation of the final circuit at tt corner is given as Fig.3, from which it is seen that the design of the circuit fulfill the design request.

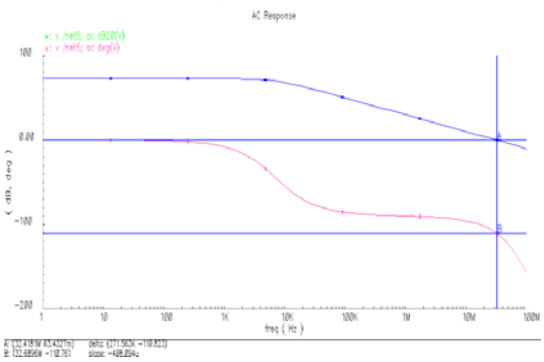

Fig.2 ac simulation of the amplifier

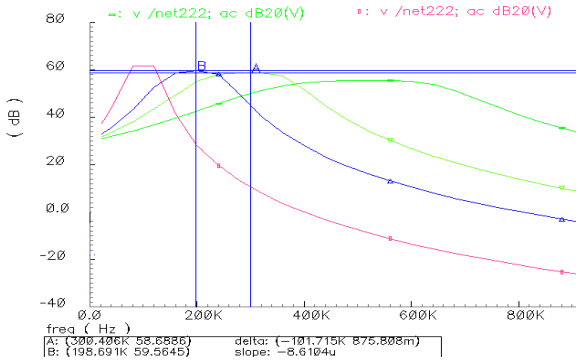

Fig.3 ac simulation of the complex filter

3. Design of automatic calibration system

The bandwidth and the center frequency of the active RC complex filter are decided by resistors and capacitors, both values of which are easily influenced by temperature and process [11], bringing in the distortion of the center frequency and bandwidth. In order to reduce the distortion, the resistor arrays used in the filter are controlled by automatic calibration system to make sure that however the process and temperature changes, the multiplier of RC, as well as the center frequency and bandwidth, stay the same value. There are two methods of calibration, front calibration and background calibration, according to the order of the calibration. On the consideration of low power design, this paper takes the measure of front calibration system shown as Fig.4, which is made up of RC oscillator

circuit and digital module.

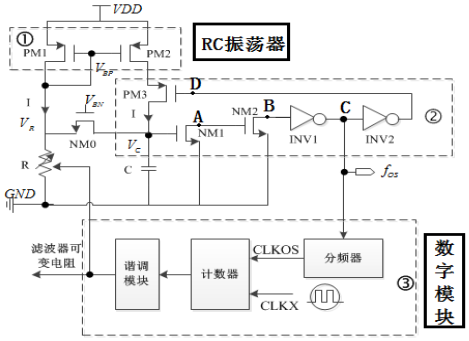

Fig.4 Schematic diagram of RC calibration system

3.1 RC Oscillator Circuit

The RC oscillator circuit shown in Fig.4 is made up of a self-oscillator circuit, a current mirror circuit and left comparison section. The self-oscillator circuit provides the needed current I and the bias voltages, V_{BN} and V_{BP} of the total circuit. And the mirror circuit, copying the current of the resistor R to the capacitor branch to provide current for the capacitor to charge or discharge, could be simplified to the part shown as ① in Fig.4. In the comparison section given as ② in Fig.4, when the voltage V_C across the capacitor is higher than the threshold voltage, namely $V_C \geq V_{GS1} - V_{TH1}$, MOS NM1 turns on, then the voltage of point A turns down and the MOS NM2 turns off, resulting in the voltage of point B to turn high. After inverters INV1 and INV2, the voltage of point D turns high and the MOS PM3 turns off, thus the capacitor will discharge to variable resistor R through the MOS NM0. On the contrary, when $V_C < V_{GS1} - V_{TH1}$, NM1 turns off and the capacitor will be charged by current through PM3 from PM2. When the capacitor is charged and discharged continuously by the oscillator, the output signal will be square wave signal with the frequency of f_{OS}.

During the charging and discharging time of Δt, the changing voltage of the capacitor is ΔV_C. Supposing that the current flowing through PM1 is I, the current flowing through PM2 is I as well under the influence of the current mirror. The variable parameters meet the function below.

$$\Delta V_C = \frac{I \bullet \Delta t}{C} \tag{2}$$

The voltage across the variable resistor R is V_R, then

$$I = \frac{V_R}{R} \tag{3}$$

From function (2) and function (3),the function (4) is easily known.

$$\Delta t = RC \bullet \frac{\Delta V_C}{V_R} \tag{4}$$

The charging and discharging cycle time of the capacitor is obtained as function (5).

$$T = 2\Delta t = 2RC \bullet \frac{\Delta V_C}{V_R} \tag{5}$$

The frequency of the output signal of the RC oscillator is given as function (6).

$$f_{os} = \frac{1}{T} = \frac{V_R}{2RC\Delta V_C} \tag{6}$$

3.2 Digital Automatic Calibration Module

The digital automatic calibration module is parted into two sub-modules, the frequency counting module and the comparison module. The output signal of the RC oscillator is divided by two. Taking the stable square wave *CLKX* generated by crystal as a standard, the signal *CLKOS* divided from the output signal of the oscillator is counted and ratio *N* between *CLKOS* and *CLKX* fulfill the

function $f_{os} = \frac{N \bullet f_X}{2}$. In the comparison module, the control to the resistor array is implemented by comparing f_{os} and the reference signal f_{REF}.

The frequency of the reference signal is 32 kHz, the simulation at the corner of tt/ff/ss is given as Fig.6. From the figure, it is seen that the output frequencies of the 3 different corners are 32.10 kHz, 32.38 kHz and 31.26 kHz. The error is less than 2.5%.

4. Simulation result and layout

The circuit is simulated on SMIC 130nm. It is demonstrated that the calibration succeeds and the control code of the resistor array will be saved in the register after finishing the automatic calibration process. Then when the complex filter starts to work, the code will be sent into successfully and the calibration of the filter will be complemented. As an example of 300 kHz mode, the simulation curve is given as 1 in Fig.5 with the center frequency of 300 kHz and the bandwidth of 278 kHz, satisfying the design request. If the circuit isn't calibrated, the curves of the ac simulation on ss and ff corners will be 2 and 5 in Fig.5 with the error of the center frequency more than 50%. On the contrast, the error will be less than 1% after the calibration with the curves shown as 3 and 4 in Fig.5. The circuit works on the supply voltage of 1.5V and the current of less than 500uA, that is to say, the total power consumption is less than 0.75 mA.

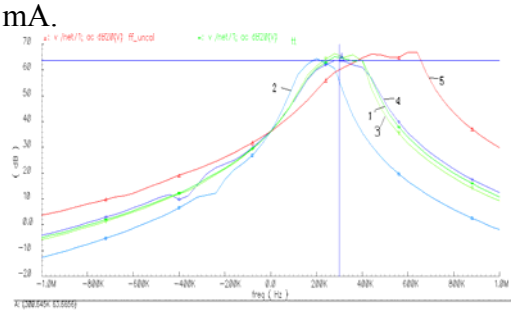

Fig.5 ac simulation of the filter on 300 kHz mode

The contrast of the power consumption, the orders and the image rejection of the complex filters shown in different paper are given in list 1, from which it is easily seen that the complex filter proposed in this paper has the advantage of multi-passband and low power consumption.

Table1 Contrast of the results

	This paper	reference[3]	reference [4]	reference [5]
Power(mW)	0.75	1.16	2.77	14.22
Order	3	3	12	7
Image rejection(dB)	45	47.5	71	98
Passband amount	4	1	2	1

Fig.6 shows the total layout of the chip with the total area of 3.4mm*3.4mm. In the center of the layout is the complex filter and the upper part, shown as rectangle 1, is the analog circuit, namely RC oscillator circuit. The left and the bottle part is the digital module of the chip, which contains the digital automatic calibration system of the filter.

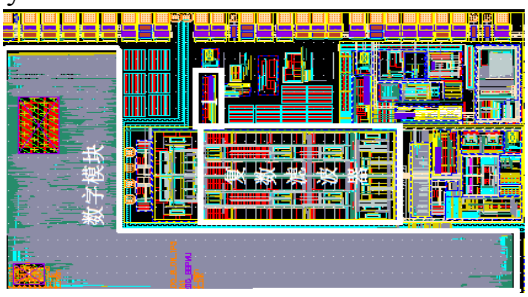

Fig.6 Layout of the total chip

5. Summary

A low power design of complex filter with 4 pass bands has been proposed in this paper. All of the capacitor arrays used in the circuit have the structure of miller compensation to solve the problem of

instability resulting from multi-band and multi-poles. In order to compensate the difference of the center frequency and bandwidth generated by the process, an automatic calibration system made up of a RC oscillator and digital module has been present. The complex filter shown this paper works at the current less than 500uA at the supply voltage of 1.5V while its image rejection reaches more than 40dB and the difference is less than 1%, applying for RFID chips properly. The filter have 4 pass bands, which means wider application prospects.

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