The Design of Configurable TFT-LCD Controller Based on Nios II

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Abstract. To solve the problem that different types of LCD screen have different drivers,this paper puts forward a design method based on embedded software core. It constructs LCD controller IP core and Nios II embedded softcore processor on SOPC. It uses C language to realize video sync,the conversion, caching and transmission of pixel data and image display. The design method is simple, fast, and has strong portability and wide applicability. The results show that this design scheme of LCD controller is reasonable, the operation is stable and the pictures display clearly.

Introduction

As the characteristics of small size, flat-panel, no radiation, low power consumption and digital interfaces, LCD(Liquid Crystal Display) have been increasingly widely used in portable embedded products, which has a very broad market prospects. However, the standards are not uniform because there are many LCD screen manufacturers. What's more, LCD screens of different manufacturers often can not connect with general LCD controller seamlessly. The prices of timing chips specially designed for LCD panel that the manufacturers recommend are high, and the external interface logic need to be redesigned. In order to maximize solve the above problems and achieve the design goal on single chip system, this paper uses Nios II embedded soft-core processor and LCD controller IP(Intellectual Property) core based on SOPC(System on Programmable Chip) technology, which finished the design of TFT-LCD(Thin Film Transistor Liquid Crystal Display) controller with high performance on FPGAdevice.[1]

System solution. The design uses cyclone II device family EP2C35F484C8N produced by Altera Company. This chip has 3,326 configurable logic cells and 475 user pins,which not only meets the design's requirements and also has great headroom.We uses AT070TN83, a type of TFT-LCD, which s produced by Taiwan's Chi Mei Electronics Company.The resolution is 800 × 480. It has 18 bits of color signal (each of R, G, B is 6 bits). It has four control signals: hsync, vsync, enable and the scan clock.

The purpose of this design is to display image on the TFT-LCD. Building SOPC hardware system on FPGA chip, including FLASH controller, SDRAM controller, TFT-LCD controller, SG-DMA module and the FIFO module. The flash is used to store hardware configuration, implementation program, and image data. At first, hewing out image frame buffer in the SDRAM, then storing an image data into the buffer, and at last using Scatter-Gather DMA to send image data from SDRAM to TFT-LCD Controller and display it. The diagram of this scheme design is shown in Fig.1.

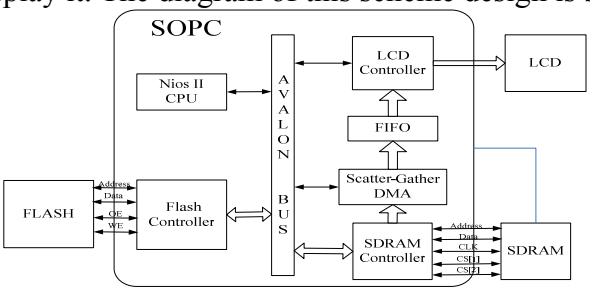
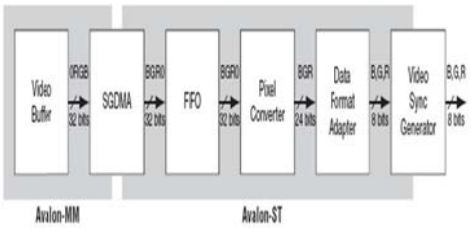


Fig.1 Systemdesign

On-chip Controller Design.SOPC is a flexible and efficient solution.It integrates many functional modules required in system design such as processors, memory, I/O port, custom peripherals into a

FPGA chip to form a programmable system on chip. It uses framework "microprocessor + programmable logic". The users can easily add IP core in the system to realize the system on a chip that has specific functions and is easily configured and expanded.[2]

TFT-LCD Controller Principle.Altera provides the video sync generator core and the pixel converter core in SOPC Builder, which are shown in Fig.2. The video sync generator core receive pixel data stream in RGB format,and output them to the off-chip display in appropriate timing sequence. You can configure the core to support different TFT-LCD with different resolutions and synchronization timing sequences. The pixel converter can transfer pixel data according to the format that video sync generator requires.[3]



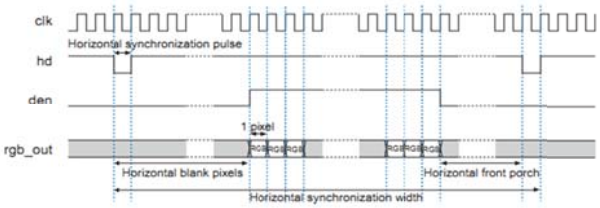


Fig.2 TFT-LCD ControllerFig.3 TFT-LCD timing sequence

The parameters of Video Sync Generator Core can be configured to support multiple pixel formats and custom color depth mode, and support monitors with different resolutions. Pixel data can be output 8 bits at three times and it can also be output 24 bits at one time. In order to adapt the design requirements of TFT-LCD, the timing sequence uses the format of output which is shown in Fig.3.

TFT-LCD Controller Implementation.The design builds TFT-LCD controller by calling the IP core of SOPC, which is shown in Fig.4. The controller includes Scatter-Gather DMA Controller, FIFO, Avalon-ST Timing Adapter, Pixel Converter and Video Sync Generator.

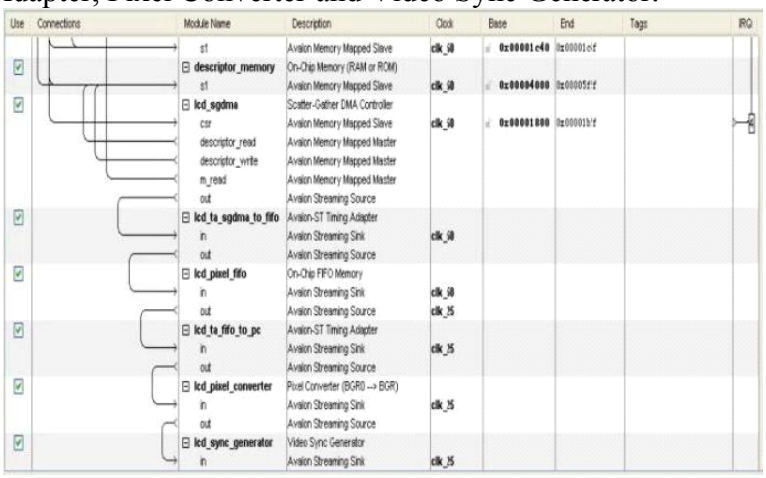
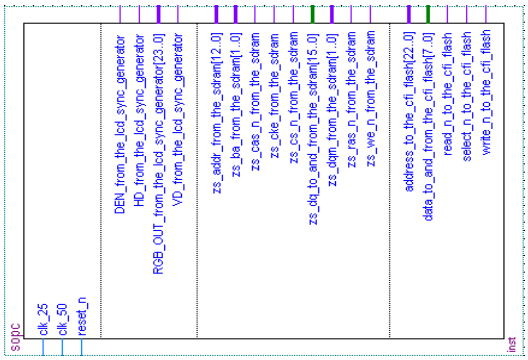


Fig. 4Hardware structure of system

SG-DMA (Scatter-Gather Direct Memory Access) Core is used to achieve high-speed data transmission between two SOPC components. It is different from DMA that SG-DMA can move data stored in non-contiguous address space to contiguous address space, and vice versa. Asynchronous FIFO is used as buffer for pixel data.

Pixel data of image buffer is 4 bytes , that is 0, R, G, B, but the pixel data that video sync generator receive is 3 bytes of RGB. So, it is necessary to remove unused byte of per pixel data by pixel converter lcd_pixel_converter.After building the SOPC system, compile it and then generate hardware system module in QuartusII,which is shown in Fig. 5.



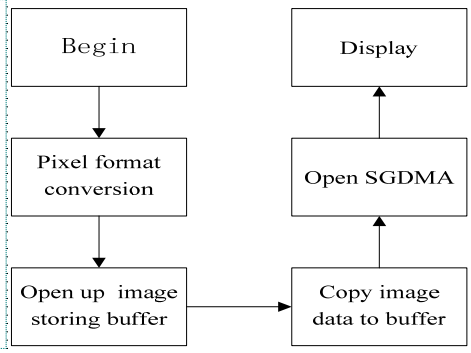


Fig .5 Hardware system moduleFig.6 The program flow chart

Procedure Design. Nios II embedded soft-core processor is a SOPC solution provided by Altera. Nios II is a general RISC (Refined Instruction Set Computer) using pipeline technique and harvard architecture,and it is configurable.It combines a wealth of peripherals, special instructions and hardware acceleration units which can provide extremely flexible and powerful, low cost SOPC system. The developers need to integrate them according to their practical needs.The LCD driver combining with Nios II, you can get an extensible, general purpose IP cores,which can solve the problems of different drivers among different types of LCD.[4]The program flow chart of this design is shown in Fig.6.

Pixel Data Format Conversion.The format of pixel data extracted by software is3-byte RGB, while per data that SG-DMA reads is 32 bits. So, at first, the original pixel data should be transformed into 32-bit, that is 0, R, G, B format in order to prevent dislocation when reading.The conversion procedure is as follows:

```
s_row = s;d_row = d;
for(r = 0 ; r < a_hgt ; r++ )
{
  s_row = s;d_row = d;
  for(c = 0 ; c < a_wd ; c ++ )
  {
    *(unsigned char *)(d_row + 2)   = *(unsigned char *)(s_row);
    s_row += 1;d_row += 1;
    *(unsigned char *)(d_row)   = *(unsigned char *)(s_row);
    s_row += 1; d_row += 1;
    *(unsigned char *)(d_row - 2)   = *(unsigned char *)(s_row);
    s_row += 1;d_row += 1;
    *(unsigned char *)(d_row)   = 0x00;
    d_row += 1;
  }
  s+= s_incr;d += d_incr;
```

Open up image storing buffer.Calling for system functionmemset(),which is included in header file string.h.

```
memset( (void*)(display->buffer_ptrs[display->buffer _written]->buffer),
    0x00, display->bytes _frame );
```

Copy Image Data to Buffer.o copy 32-bit pixel data into the display buffer of SDRAM, theprocedure is as follows:

```
int copy ( char* d, char* s,
           int wid _d,
           int wid _s, int hgt_s )
{
  int z;
  for ( z = 0; y < hgt_s; z++ )
```

```
    {
      memcpy( d, s, (wid _s * 4 ));
      s += (wi _s * 4 );
      d += (wid _d * 4 );
    }
  }
```

Pixel Data Transmission.Opening the SG-DMA and configuring it, it will transfer image data to TFT-LCD controller.Corresponding program is slightly.

Image Display.The TFT-LCD controller is constructed by hardware logic cells of FPGA, so it does not need to be controlled by cpu of Nios II embedded soft core system.

Debug and Simulation. This design uses Quartus II embedded logic analyzer SignalTap II to simulation and test. The full name of SignalTap II is SignalTap II Logic Analyzer, which is the second generation system level debugging tool that can capture and display real-time signal, observing the interaction between hardware and software of system.[5]The simulation result is shown in Fig. 7.

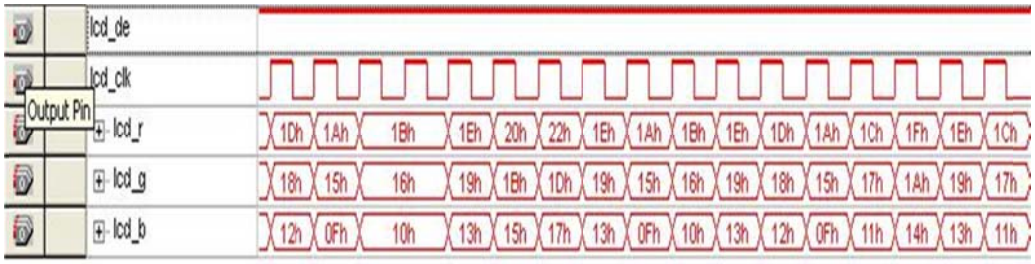


Fig. 7 Simulation result

Conclusion

This paper presents a software and hardware combination design method to design TFT-LCD controller based on SOPC Builder and Nios II of FPGA. It solves the problem of difference among different types of LCD drivers,builds up LCD controller IP core and Nios II embedded soft-core processor,uses C language, to realize video sync, pixel data conversion, cache,data transmission and display. The design method is simple, fast, portable, and widely applicable. The results show that through configuring parameters of IP core in SOPC Builder,it can meet displays with different timing and resolution,which enhance flexibility and portability of this design.The result has been completed in hardware testing.

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