Data Acquisition and Display System Based on FPGA and ARM

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Abstract. Based on FPGA and ARM, this embedded system of data collection, measurement and display is designed to tackle problems like bad real-time capability, limited data storage and low transmission rate of signal collection in electronic measurement. FPGA is used to control A/D and DDR2 storage chip to fulfill large data collection and storage. Control signal interaction in FPGA and ARM system is obtained through SPI trunk. Then use the DPRAM core in Quarter to upload data. Finally we can use Qt program on the Linux to display the data with graph and measure signal parameter. According to the experiment results, This system can be applied to collect, store, transfer and display large data. The display is reliable and the error meets the expectation.

Introduction

Data acquisition is an important link in the process of signal processing [1], traditional data acquisition is mostly designed based on microcontroller, which, to a certain extent, restrict data acquisition and transmission speed rate, the sequential control precision and the storage capacity etc, in particular when there is hard requirement on the real-timing of acquisition system and data storage volume, normally it is very difficult to fulfill design requirement [2,3]. With the rapid development of EDA technology and embedded technology, the design framework taking FPGA and ARM served as controller, externally connected with high transmission speed and high capacity DDR2 memory, has provided a good solution for problems that the traditional data acquisition and display system is not competent in some acquisition occasions requiring real-timing, high speed rate and high storage capacity. This design framework is characterized by high speed rate, high level of integration, low energy consumption, low cost and high storage capacity etc.

In this paper, EP3C40F780C6 instrument of Cyclone III series from Altera and ARM1 chip S3C6140 built embedded platform from Samsung Corp was applied, using 16 bit high precision analog digital conversion chip AD9269 to complete the data acquisition, two DDR2 SDRAM chips MT47G256M8 is used as data cache memory, data acquisition and storage capacity is up to 512MB. By building embedded Linux software platform and GUI graphical interface using Qt/E embedded version developed by Nokia, it will not only be featured by excellent cross-platform, object-oriented, rich API provision, but also providing a large number of development file.

Overall architecture of system

The overall architecture of the system is shown in figure 1, primarily consists of analog front end, signal acquisition storage and control part as well as embedded ARM. Analog front end mainly implements signal input mode, measurement range shift selection and signal conditioning function etc, to reduce the impact of different shift on signal bandwidth and amplitude, the analog front end uses passive attenuation network, impedance variation, post-stage amplifying and ADC drive circuit etc to optimize the input signal; the signal acquisition storage and control part mainly implements read and write of DDR2 SDRAM memory data and the interaction of instruction and data between

FPGA and ARM; while the embedded part mainly implements various external interfaces of system and the operation interface of Qt graphic application program etc.

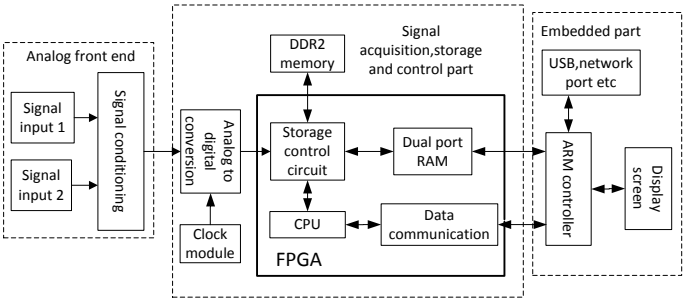

Figure 1 Overall block diagram of system

Function Design

System function design is shown in Figure 2, the main function is to implement parameters configuration, acquisition control, waveform display and measurement as well as access of waveform data file etc.

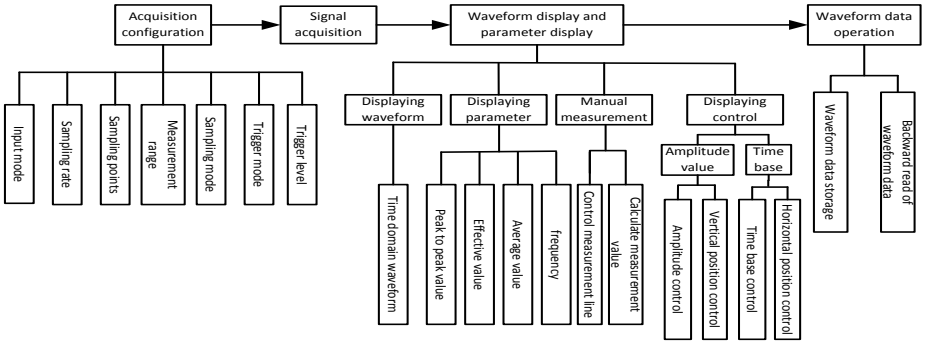

Figure 2 block diagram of function

Parameters configuration, data acquisition, backward reading and other instructions is sent in the form of frame to FPGA through the SPI bus from the application program, and then through FPGA control circuit to complete parameters configuration, data acquisition and data backward read control. Frame structure is defined in Table 1, including frame head, frame length, instruction type, data segment, CRC calibration and frame tail, the data segment length thereof is variable according to the specific instruction. The frame instruction type of system configuration is defined as: 0x00, its data segment is defined in table 2; FPGA after receiving one frame data from application program will analyze the instruction type and data segment parameter etc, then, call corresponding function to complete configuration according to the instruction type and its carrying parameter information. For other instructions, such as data acquisition instruction and data back read instruction, they are similar with configuring frame instruction.

Table 1 frame structure

Frame head:0x5A	Frame length	Instruction type	Data segment	CRC（Optional）	Frame tail: 0xA5

Table 2 configuring frame data segment

Input mode	measurement range	Sampling rate	Number of sampling point	Acquisition mode	Trigger level	
					High level	Low level

For the collected data, after being calculated, signal peak to peak value, effective value, average value and main frequency component can be derived. Finding the maximum and minimum values of the voltage in the collected data, the difference of between them will be the peak to peak value of the input signal. The effective value and the average value of the signal can be derived respectively from formula (1) and (2).

$$V_{rms} = \sqrt{\frac{\sum_{k=1}^{N} v_k^2}{N}} \quad (1)$$

$$V_{mad} = \frac{\sum_{k=1}^{N} v_k}{N} \quad (2)$$

In the formula, V_{rms} is the effective value of the signal amplitude; V_{mad} is the average value of the signal amplitude; v_k is the voltage value of the signal, k thereof equals to *1*,*2*,*3*…*n* (*n* refers to the number of sampling point).

At present, we have already studied a variety of frequency measurement algorithms, the algorithm based on Fourier transform has a strong filtering and anti-interference performance [4], so in this paper, FFT analysis algorithm is applied, through FFT algorithm operation on the collected data to obtain the primary frequency of the signal. In order to make the waveform display more flexible, knobs, keys and other control elements are designed in the interface, to achieve movement and zooming of waveform in the vertical and horizontal direction. Additionally, the system is also equipped with the function of waveform data preservation and recurrence, through external interfaces of system such as USB, network port etc. to accomplish copy and write of the data file.

Hardware design

Design of analog front end of signal

The system is required to realize both AC / DC input methods and multiple measuring voltage shifts, and the voltage range thereof is up to± 40V, so, the design of the analog front end becomes an essential part to the system. In order to ensure different measuring range and input mode, the amplitude of the input analog signal is conditioned into the ADC suited input range, the design of analog front end primarily consists of passive attenuation network, impedance variation, post stage amplifier and ADC drive circuit.

Because the input voltage range required by the system is up to ± 40V, which exceeds the dynamic range of most active devices, and makes the post-stage impedance variation and signal conditioning more difficult to process. It is necessary to implement passive attenuation to the large signal at the input end; passive attenuation generally uses resistance voltage division. However, in the actual circuit, at low frequency, resistance voltage division can well realize rated voltage ratio equal to resistance ratio. But for high frequency input signal, the resistance is not an ideal resistance model, parasitic component can often occur. Therefore, paralleling a proper capacitor nearby the divider resistance can well realize voltage division ratio irrelevance of the frequency, this system uses relay to implement different input mode and shift, after that, switch the signal to the corresponding channel of the attenuation network for the post processing. The system has 1MΩ input impedance, to improve the post-drive ability, an emitter follower is added between the forestage and the post-stage, effectively isolate the impact between the forestage and the post-stage. The signal after being isolated will go through post-stage amplifying and ADC drive, convert the single end input signal into differential signal suitable for ADC input range, which will effectively inhibit the introduction of noise.

Analog to digital conversion design

Low cost and low power consumption conversion chip AD9269 [5] produced by company AD is used for the system, this chip is an analog to digital converter with double channel, 16 bit resolution and the highest sampling rate up to 20MSPS, supplied by 1.8 V power supply with multi-level differential stream line structure, which can provide both unipolar and bipolar input mode. AD9269 can achieve 16 bit resolution, at highest data speed rate, it can be guaranteed that there is no missing code within the entire working temperature range, which can fulfill the requirement under various high precision application.

AD9269 in this system adopts 20MHz differential coded clock, externally connected with 1V reference voltage, the analog signal is input differentially, try every effort to inhibit the introduction of noise, the digital signal is output in shifting binary format. The input signal after being processed by analog front end circuit is converted into differential signal between -1V and +1V, then converted to digital signal for output by analog to digital converter.

Dual port RAM design

The data transmission between FPGA and ARM is realized by dual port IP core in II Quarters. Dual port RAM has two sets of mutually independent data cable, address line and control line, it can implement read and write operation simultaneously, with this unique performance[6], dual port RAM in this system served as the data communication interface between FPGA and ARM can complete high-speed transmission [1]of mass data.

The address line of SROM controller in S3C6410 of ARM11 chip, the chip selection line Xm0CSn, output enabling line nOE and data cable DATA of the system generated read sequential is very similar with the read sequential required by the driving the dual port RAM. Therefore, connect the ADDR of SROM controller and DATA signal line respectively with the read address line raddress and data cable q, in the meantime, connect the signal line Xm0CSn and nOE of SROM controller after being connected with inverter respectively with the enabling line rden and read clock line rdlock, as shown in figure 3, this may facilitate to drive dual port RAM to complete data access operation.

Dual port RAM plays a very important role in the system data transmission. The system configuration is completed and after receiving the acquisition instruction, analog to digital converter will write the collected data to the DDR2 memory, in this moment, the dual port RAM is in idle status. When FPGA receives backward read instruction sent by ARM, requesting taking data from the dual port RAM, FPGA will read out part of data in the DDR2 memory, and write in the dual port RAM at the same time, when dual port RAM is fully written, inform ARM to read the null data from dual port RAM, and then write data to dual port RAM, cycle until ARM taking all the data in DDR2.

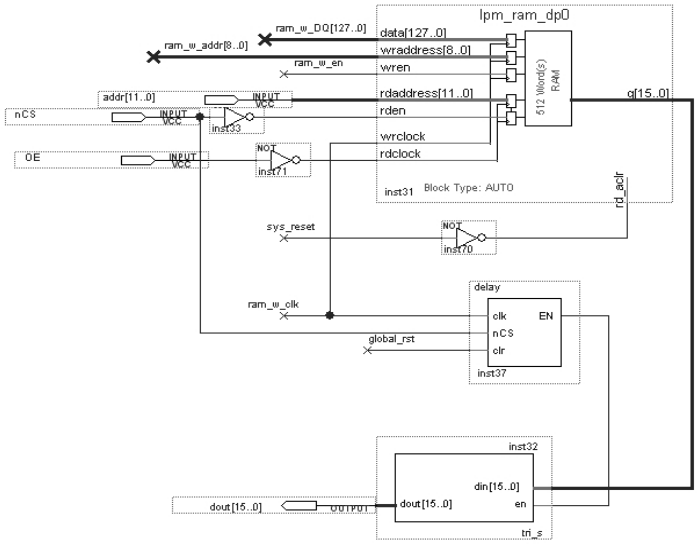

Figure 3 dual-port RAM and ARM interface module connection diagram

Software design

Building embedded Linux operation system software platform

Linux was first founded in 1991, invented by Linus Torvalds from Finland; it is now developed into a stable operation system with rich functions. Embedded Linux is a transplant of standard Linux onto embedded system, featured by open source code, high performance, tailorability and powerful network function; it is widely used in embedded system. Embedded operating system normally consists of four parts: Boot-loader, kernel, file-system and user application program. The first three parts thereof is to ensure the normal operation of the Linux, it is also a precondition for running user's application ,such as Qt, etc.

This system has successfully transplanted uboot1.1.6 and kernel Linux3.0.1 and fabricated yaffs2 file system. By testing, it is known that Linux system can be started and operated normally.

Implementation of SPI serial communication between ARM and FPGA

To realize the transmission and response of instruction frame between Qt application program and the FRGA, the communication of ARM and FPGA should be implemented. SPI is full duplex synchronous serial bus developed by Motorola, its interface is composed by four signal cables namely MISO (serial data input), MOSI (serial data output), SCK (serial displacement clock) and SS (slave enabling signal), it is a kind of communication bus working in master/servo mode featured by high speed, full duplex, synchronization, based on these excellent performances, selecting FRGA as SPI servo and ARM as SPI master to realize transmit-receive of frame data. Because 32-bit Nios II soft core microprocessor developed by Altera was constructed in FPGA, the peripheral configuration of this microprocessor contains SPI bus controller, so, only with simple configuration, SPI slave design can be realized. Linux operating system can not directly communicate with the peripheral interface, so it is necessary to write SPI serial port driver as a bridge between the operating system kernel and the peripheral of SPI serial port. In the operating system kernel, the bottom serial port peripheral is abstracted as the form of the device file [7]. In Linux, using spi master structure of code listing 4.1 to describe the controller deriver of one SPI master, the main members are the serial number of the master controller, chip select number, SPI mode and the functions used for setting clock as well as the function used for data transmission. The SPI master controller driver of S3C6410 in this system is located in the driver/spi/spi_s3c.h and driver/spi/spi_s3c.c, mainly to realize functions of setup () and transfer () of spi_master etc [8].

Code list 4.1

```
structspi_master
{
struct device dev;
s16 bus_num;
u16 num_chipselect;
int (*setup)(struct spi_device *spi);
int (*transfer)(struct spi_device *spi,
struct spi_message *mesg);
void (*cleanup)(struct spi_device *spi);
};
```

Realization of Qt graphic application program

Qt/E graphic display implementation architecture

Qt/E i.e. Qt embedded is a graphic interface development tool developed by the Norwegian Trolltech, it can directly interact with Linux I / O and Framebuffer via Qt application program interface, characterized by high operation efficiency and with object-oriented programming, and it owns good architecture and programming mode. Please see figure 4 for its implementation structure.

<table>
<tr><td colspan="2">Qt/Embeded application program</td></tr>
<tr><td colspan="2">QWSServer graphic event service</td></tr>
<tr><td colspan="2">Qt/Embeded</td></tr>
<tr><td>Framebuffer</td><td>Input device drive</td></tr>
<tr><td colspan="2">Linux operation system</td></tr>
<tr><td colspan="2">Bottom layer hardware platform</td></tr>
</table>

Figure 4 Qt/Emeded implementation structure

The bottom layer of the Qt/Embedded abandons Xlib, using FrameBuffer as the bottom layer graphic interface. FrameBuffer is a driver interface, abstracting the display device as a frame buffer area, meanwhile abstracting the external input device as mouse and keyboard or other input events; this will ensure that the bottom layer interface will support the mouse, keyboard, touch screen and the user defined devices. As for users, there is no difference between FrameBuffer and other device drivers under Linux, the user can regard it as a virtual memory, you can either read data from this memory, or write data to this memory, the data that is written shall be reflected immediately in the display interface[9]. In order to enable Qt/E to run in the embedded Linux system, the system kernel must support FrameBuffer.

Interface design of Qt

System Qt program interface mainly includes acquisition configuration, waveform display, parameter display, amplitude and time base control, parameter measurement, waveform data processing and key control part, please see figure 5 for design interface.

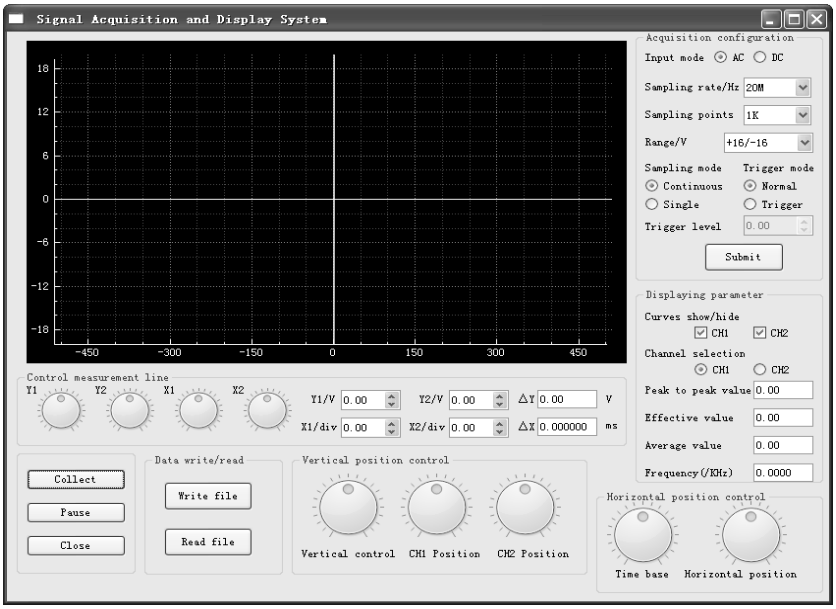

Figure 5 display interface

The acquisition configuration part mainly implements parameter configuration such as system input, sampling rate, sampling points, measurement range, acquisition and trigger mode etc, configuration frame is formed after completing configuration control element operation, SPI bus between system interior ARM and FPGA is to complete interaction of configuration information; In the waveform display area, display of waveforms of two ways and the measuring auxiliary line shall be completed by calling the Qt program; the peak to peak value, effective value, average value of the waveform of two ways and the frequency are displayed in real time at the parameter display area; the amplitude and time base control area mainly implements movement and zooming of waveform in horizontal and vertical direction, making the collected waveform easier for observation and measurement; measurement and control part is to control the waveform measurement auxiliary line, thus to facilitate user's manual measurement of waveform; moreover, the interface is also designed

with the function of waveform file preservation and data backward read. Please see figure 6 for program design flow.

Preservation and backward read of waveform data file

QDir, *QListWidgetItem*, *QFile* and *QTextStream* and other operation related category are provided in Qt, facilitate the read and write of waveform file.

```
QFile f(readWritePath);  //file read and write route
QTextStream txtInOutput(&f);  //define QTextStream variable
f.open(QIODevice::ReadWrite);  // open file
txtInOutput<<buf_AA[I]<<','<<buf_BB[i]<<endl;  //write collected data to file
QString lineStr= txtInOutput.readLine();  //read the data of file line by line to QString variable.
```

The above example code specifies the route for file read and write, and gives the method of file read and write operations. In order to distinguish the data collected at different times, the file is named by plus the current time tag and size of data for file storage, for example: the file is named as "*adc_2015-11-20_21-45-12_1K*", its example code is shown below.

```
current_date_time = QDateTime::currentDateTime();  //acquiring current time of the system
current_date=current_date_time.toString("_yyyy-MM-dd_hh-mm-ss");  //define time format
write_filename=sourceName+current_date+"_"+QString::number(size_nk,10)+"K";
```

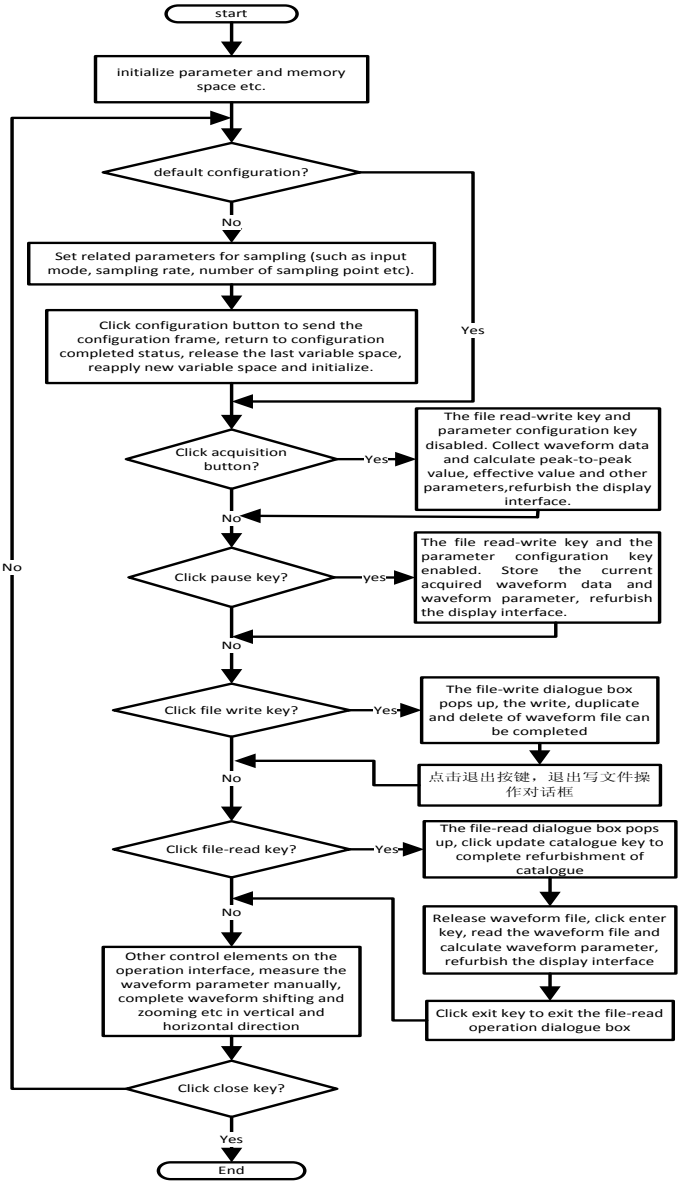

Figure 6 program flow chart

Test result

Through practical test, the system may accomplish single / continuous acquisition, triggering, waveform parameter measurement, display and other functions for the amplitude between -40V and +40V and low and medium frequency signal, the preservation and copy of data file is normal, the work is stable and reliable, the interface can be operated easily with clear display, various indicators have met the design requirement. Experimental verification is shown in figure 7.

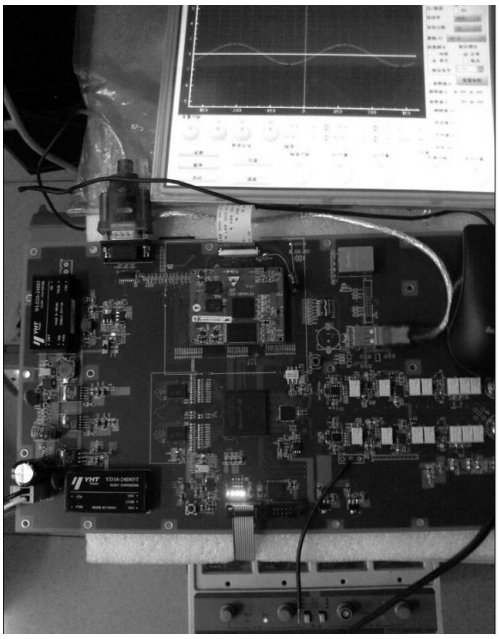

Figure 7 physical body of system

Conclusion

The data acquisition and display system introduced in this paper fully utilizes FPGA performance of high-speed processing and signal transmission, as well as the high storage and transmission capacity of DDR2 SDRAM, which is competent to complete quick acquisition and transmission of mass data. The design of analog front end of signal has effectively achieved switch of different shift, while ensuring the signal bandwidth meet the design requirements. The test shows that the data acquisition, display and storage scheme based on FPGA and ARM architecture is feasible, the circuit is reasonable designed with strong reliability.

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