Research on FPGA-based SCU Software Output Signal Testing Technology

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Abstract: SCU and its software are widely used in both electrical and electronic devices. It is important and difficult to conduct quantitative analysis, accurate measurement and quality evaluation in SCU circuit design and manufacturing. In order to solve the problem of SCU-based circuit signal testing, this paper mainly studies the FPGA-based SCU output signal testing technology, testing requirement and test case analysis method, etc.

Introduction

As device informationalization and intelligence rapidly develop, Single-Chip Microcomputer (SCU) and its software find increasingly wide spread application featuring more complex structure, higher requirements for software testing and larger task difficulty. This research is carried out in order to update device software testing and evaluation technology, improve software technology analysis and evaluation standards and meet the requirements for device software development.

FPGA-based SCU software output signal testing adopts in-series FPGA structure and Field Program able Gata Array(FPGA) is taken as the bridge between SCU and computers to maximize real-time display and accurate measurement of SCU output signals such as control feedback and sequence signals; on the basis of online programming characteristics of FPGA, the method for acquisition of digital level signal, analog signal, sequence signal, energy signal and encoding signal is constructed modularly to maximize accurate measurement and real-time display of SCU testing data.

SCU software output signal testing requirements involve digital level signal, analog signal, sequence signal, energy signal and encoding signal, etc.; these signals vary greatly, among which the sequence signal is the most typical. Based on the characteristics of diversity in the type and sequence of SCU system signals, a genetic algorithm (GA) based method for creation of testing models and requirements is constructed. A complete signal testing method model and testing signal requirement coverage statistics are developed based on small sample testing data of SCU system observation to make a quantitative analysis on SCU software testing requirement coverage rate and test case adequacy. The method for analysis of testing requirements and test cases is mainly to divide problem domains of input/output signals, destruct input/output signal combination to gene expressions, build small sample signal data-based fitness functions, adopt the genetic selection algorithm for intelligent searching for SCU input/output signal problem domains and boundary conditions and provide quantitative analysis results of testing requirement coverage rate for different testing plans and test case adequacy to testing personnel for comparative analysis.

Testing Output Signal Display Technology

In some testing process of the SCU, signal acquisition requires real-time display. Based on the diversity of SCU system signals, the acquisition system must adopts relatively high transmission rate and flexible channel selection and sampling method. As FPGA is programmable online, the above requirements can be realized by the FPGA hardware and internal configuration of FPGA can

be flexibly modified based on specific testing conditions. FPGA is used for realization of master control logical module. The Data acquired by the SCU is saved in the FIFO (First In First On memory area) of FPGA which can send acquisition signals to the computer via USB based on setting of the user through systematic logic and clock operation. The Tester may select a channel, sampling frequency, SCU system and feedback signal on the soft panel designed by Labview to generate a group of commands. The computer can send the commands to FPGA via USB communication port and then FPGA would resolve the commands and control the master control logic module.

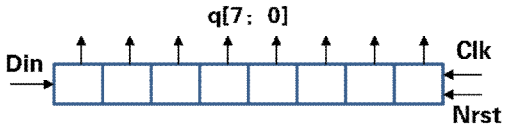

Figure 1 Deserializer Structure

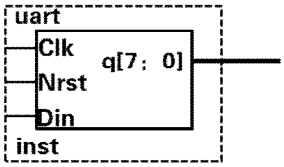

Figure 2 Schematic Diagram for Deserializer

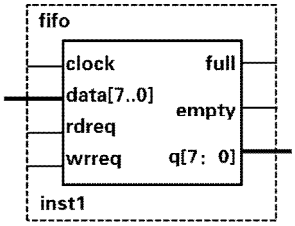

Figure 3 Schematic Diagram for FIFO Core Module

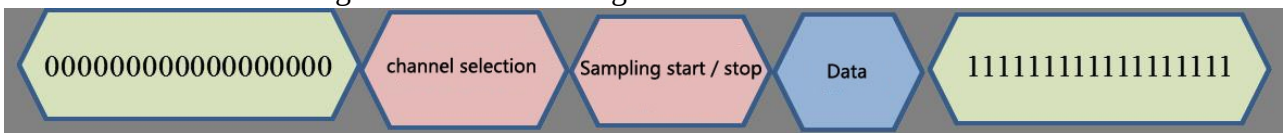

Figure 4 Format of Command Logic Transmission Data

The deserializer is designed to load the serial input data into the 8 - bit register and then perform parallel output. The structure of the deserializer is shown in Figure 1. The schematic diagram for the deserializer is shown in Figure 2. As shown in the figure, Din is serial input signal of the SCU, q [7:0] is parallel output data, Clk is converted clock signal and Nrst is reset signal. SCU output data is buffered in FIFO. An interrupt signal will be generated and sent to the computer when the memory capacity reaches the preset redundancy. Testers can set FIFO redundancy by register writing but the redundancy shall not be too close to FIFO depth in principle, for the FPGA still performs data acquisition and storage when the computer adopts USB communication and 68013 corresponding to FIFO is interrupted. If the preset redundancy is excessively close to FIFO depth, it is prone to FIFO overflow error. Signals of FIFO core module include: RW data q/date, RW enable rdreq/wrreq, RW clock clk, data null signal and full signal. Peripheral device control signals include FIFO enable, half-full, full and overflow flag signals. Schematic diagram for FIFO core module is shown in Figure 3. The FPGA can transmit the data to the computer by 72bit / frame. The data format is shown in Figure 4. The 16 bits of “0” in the front are the frame header, the last16 bits of

“1” are frame end and the middle are channel selection bits (2), sampling start and stop bit (1) and sampling data.

Testing Requirement and Test Case Analysis Method

Testing requirement and method of SCU software control input/ output signal involve digital level signal, analog signal, sequence signal, energy signal and encoding signal, etc.; these signals vary greatly, among which the sequence signal is the most typical. Each information value domain is a range of value. For control signals, each has time quantum. It is impractical to carry out a search coverage testing on the combination of value domain and time domain of each information variety. For the reason, a method needs to be established to carry out the quantitative analysis on testing requirement coverage rate and test case adequacy. Based on diversity of SCU system signal type and timing sequence, a GA-based creation method is constructed for the testing model and testing requirement. A full and complete signal testing module and testing signal requirement are built based on small sample signal data of SCU observation and model system implementation is performed by means of MALAB software. According to software testing results, this method can generate a test case model of SCU system and obtain accurate testing signal requirement of the device and testing method of reference significance based on SCU observation data. This method is universal in the aspect of testing signal.

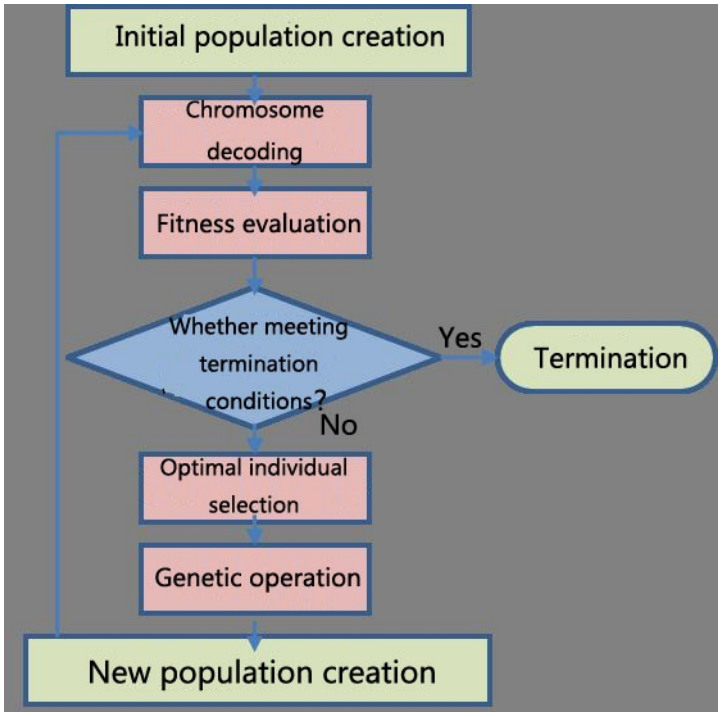

Figure 5 Flow Chart of Algorithm

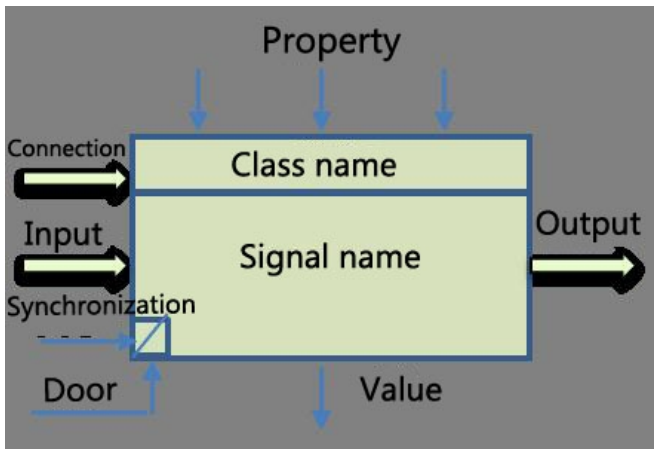

Figure 6 Signal Model of IEEE 1641 Standard Model Definition

The method for building of testing models and requirements includes determination of defined function symbol set and terminal symbol set, generation of initial population, fitness function design and selection strategy. The flow chart of the algorithm is shown in Figure 5. The function symbol set and terminal symbol set shall be closed in the genetic algorithm, that is, each function of the terminal symbol set has the same definition domain and value domain. Therefore, analog signal and digital signal cannot occur in the terminal symbol set simultaneously and any function of the terminal symbol set has no parameter. A large number of invalid data will be generated if failing in meeting the requirement. But the actual signals of the SCU are diversified, including analog signals, digital signals, protocol signals (RS232 signals and various encoding signals), so a universal signal definition and model shall be built. IEEE 1641 standard model definition is shown in Figure 5. The signal-oriented function symbol set is F={a,b,c,d,e,f,g,h,i}, in which a indicates Average operation used for calculating mean value of signal; b indicates Counter operation used for coding signal counting; c indicates Decode operation used for decoding the encoded signal; d indicates Interval operation used for calculating signal duration; e indicates Peak operation used for calculating peak value of signal; f indicates PeakNeg operation used for calculating peak-to-valley value of signal; g indicates Instantaneous operation used for calculating instantaneous value of signal; h indicates MaxInstantaneous operation used for calculating maximum value; i indicates MinInstantaneous operation used for calculating minimum value. The terminal symbol set is P={A,B,C,D,E,1,2,3,4,5,6,7,8,9}, in which A indicates sine signal, B indicates step signal, C indicates constant signal, D indicates noise signal, E indicates serial digital signal and the numbers indicate digital parameters of each signal model; initial population generation adopts crossed sample data and variation function and the sample data generates a subgroup based on equivalence partitioning. R-square is taken as the fitness calculation function and the calculation method is shown in the formula (1), where Ri indicates correlation coefficient of the ith individual with the sample set, -1≤Ri≤1; fi indicates the fitness function value of the ith individual. Ri calculation method is shown in the formula (2). Selecting operation refers to the selection from the set based on individual fitness function. The selection quantity calculation method is shown in Formula (3).

$$R_i = \frac{n\sum_{i}^{n}(T_j P_{i,j}) - (\sum_{j=1}^{n} T_j)(\sum_{j=1}^{n} P_{i,j})}{\sqrt{(n(\sum_{j=1}^{n} T_i^2) - ((\sum_{j=1}^{n} T_j))^2)(n\sum_{j=1}^{n} P_{i,j}^2 - (\sum_{j=1}^{n} P_{i,j})^2)}} \quad f_i = 1000 \times R_i^2, i = 1, \cdots, n,$$

$$N_i = \frac{N \times f_i}{\sum_{i=1}^{n} f_i}, i = 1, 2, \cdots, N,$$

Conclusions

In order to meet great-leap-forward development of device informatization and networking, software testing support method construction must be innovated to promote the conversion of software testing from the analog-based experience testing to quantitative testing-based scientific and empirical testing. The research on FPGA-based SCU output signal testing technology and analysis method of testing requirement and test case provides technical method supports for development of software systems.

References

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