"Computer organization principle" course machine concept to cultivate comprehensive experimental design

XuKunLiang[1,a]

[1]QuJing Normal University Computer science and Engineering,YunNanQuJing655011,China

[a]422078334@qq.com

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Abstract. Of this article is based on our principle experiment box designed a comprehensive experiment, the experiment unit of the input, storage unit, ALU unit, output unit five parts by line together, the experimenter as controller, constituted a set to 8 digits operation of computer system, through the experiment is complete, let the student study in separate each component on the basis of a concept of the machine.

Introduction

"Computer organization principle" is a professional computer science and technology professional foundation courses, through learning of this course, the student to the computer system basic structure, working principle of each module and the design method of the computer has a comprehensive understanding, thus forming the concept of a whole machine [1].

In actual teaching, in order to let students understand the knowledge, improve the teaching effect, the real solution "teacher difficult to teach, students learn difficult, afraid of" awkward situation, the teacher put forward many methods of teaching reform, through the network course construction, simulation experiment teaching system development stimulates the student to the interest of learning this course in order to improve the teaching efficiency [2]. Through model machine as the breakthrough point, open teaching try [3]. By strengthening theory teaching and practice teaching method [4].And based on the theory of constructivism teaching mode reform of teaching and learning role positioning [5]. The teaching method reform although has certain effect, but can make students form the concept of the whole machine. To this end, this paper design a comprehensive experiments, let the students thinking, to understand the working principle of each feature, more important is through the actual operation to make them clear that the connection between the components.

The experiment principle

Experiments involving memory, input devices, output devices, ALU several modules. These different devices to hang to the bus, through the bus can achieve information exchange, experimental block diagram is shown in figure 1.

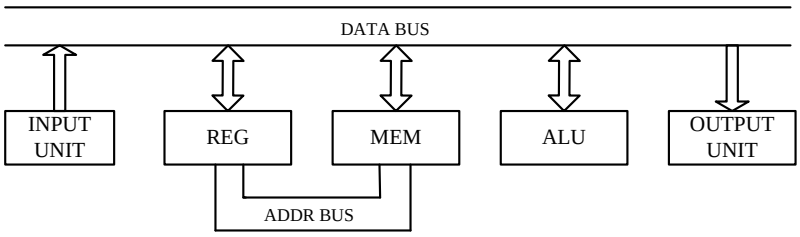

Fig.1 experimental connection schematic diagram

Experiment, to complete the operation of x + y z as an example. Data must be x, y, z through input unit by data bus into memory storage, then x and y into ALU DR1 and DR2 register to complete the add operation, operation result into the middle of the deposited in the memory to store, and then remove the intermediate results into DR1, remove the z into DR2, complete the subtraction

operation, the final results in memory. Connection diagram according to the experiment, based on the teaching experiment box ZY15Comp12BB, design get connection circuit diagram is shown in figure 2.

Diagram, arithmetic unit consists of two pieces of 74LS181 chip, ALU unit output controlled by LDPC, LDDR1, LDDR2 control to register number of DR1 and DR2, S3, S2 and S1, S0, Cn, M control 74LS181 do different operations. Memory consists of 6116 chip, 6116 CE (routing), OE (line), WE (write), with the OE grounding, often when CE = 0, WE = 0 to write operations, CE = 0, WE = 1 to read operation, CE and WE controlled by 299_G and PC_G respectively.

The operation steps

The initialization

Make the initial state of each CONTROL level is: the CLR =1, LDDR1 =0, LDDR2=0, ALU_G =1, SW_G =1, S3 S2 S1 S0 M CN = 111111299_G(CE) = 1, PC_G (WE) = 1, LDAR = 0, LDPC =1, the CLR = l-0-1, will CONTROL the switch of the UNIT SP05 state of play in the "NORM", "SP03 switch is set to" STEP "state", "SP04" switch is set to "RUN" state.

The x, y, and z respectively in the memory address of a and b, c in the cell. The concrete steps as follows:

(1)unit of input data switch place address for a;

(2)Opened the door of input three states, namely SW_G = 0, LDAR = 1 and negative pulse can be produced by press START switch T3 address into a register;

(3)The input unit data switch set to x;

(4)299 _g = 0, by making the PC_G from 1 to 0 first and then to 1 will produce negative pulse data x in the address of a storage cell;

(5)Repeating steps a-d data y and z can be deposited in the address in the b and c.

And remove the a and b cell data into ALU unit of DR1, DR2 registers. The concrete steps as follows:

(1) Switch input unit data set to take the data address for a;

(2) Opened the door of input three states, namely SW_G = 0, LDAR = 1 and negative pulse can be produced by press START switch T3 is going to take the data's address in a register;

(3) Input three states the door closed, namely SW_G = 1, 299 _g = zero can read DATA in DATA BUS unit x;

(4) LDDR1 = 1, LDDR2 = 0, produced by pressing the button PAULSE T4 is pulse data x can be deposited in the register DR1;

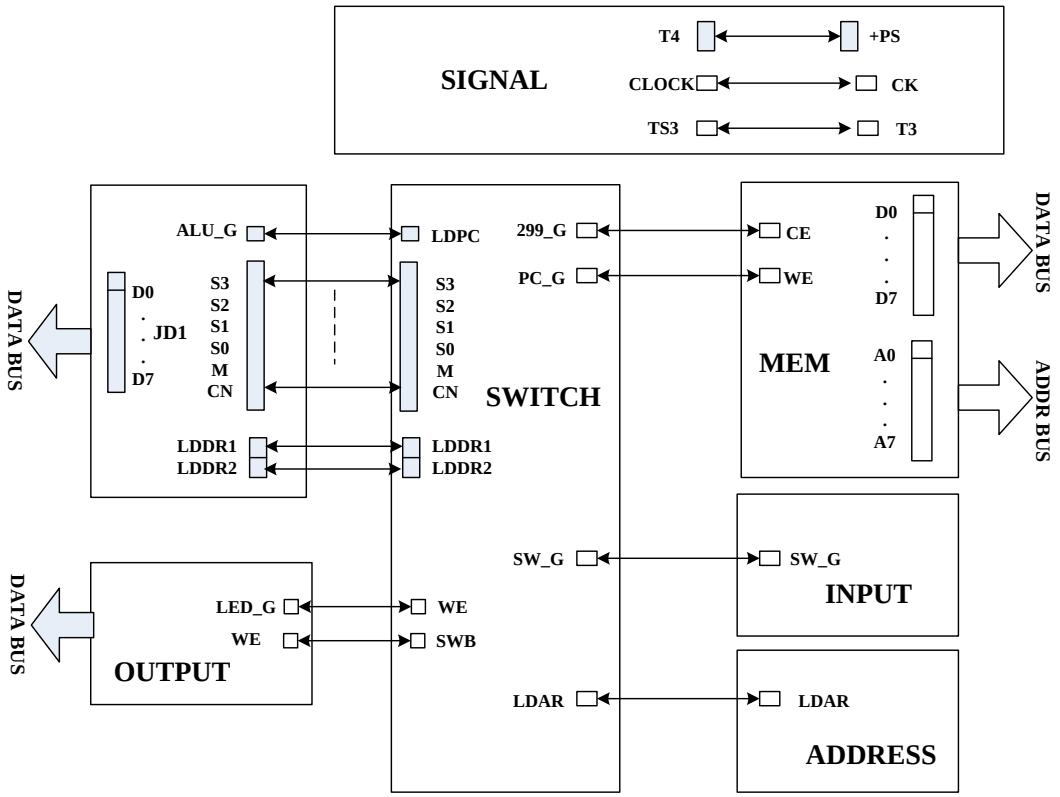

Fig.2 experimental connection circuit diagram

(5) Switch input unit DATA set to take the DATA address for b, after repeated, a. a. 3 step 2 - read DATA in DATA BUS unit can be y, LDDR1 = 0, LDDR2 = 1, by pressing the button PAULSE a T4 is impulse DR2 y DATA can be stored in registers;

x + y operation results in the address for d cell. The concrete steps as follows:

(1) The input unit data switch place address for d;

(2) Opened the door of input three states, namely SW_G = 0, LDAR = 1 and negative pulse can be produced by press START switch T3 address d in registers;

(3) Input three states the door closed, namely SW_G = 1, LDPC = 0. Buy the S3 S0 M CN = 100101 S1 and S2 can get the result of x + y in DATA BUS unit display;

(4) 299_g = 0, by making the PC_G from 1 to 0 first and then to 1 x + y will produce negative pulse data into address for d storage unit, at the same time buy LDPC = 1.

Repeat steps 3 remove d, c data unit and into ALU unit of DR1, DR2 registers. Specific operation as follows:

(1) Switch input unit data set to take the data address to d;

(2) Opened the door of input three states, namely SW_G = 0, LDAR = 1 and negative pulse can be produced by press START switch T3 will take the address of data d deposit address register;

(3) Input three states the door closed, namely SW_G = 1, buy 299 _g = 0 in DATA BUS unit to read DATA x + y;

(4) LDDR1 = 1, LDDR2 = 0, produced by pressing the button PAULSE T4 is DR1 pulse data x + y can be deposited in the register;

(5) DATA input unit "5 switch set to take the DATA address for c, after repeated.through 2 -" 3 steps in DATA can be read DATA BUS unit z, LDDR1=0, LDDR2=1, by pressing the button PAULSE a T4 is impulse DR2 z DATA can be stored in registers;

x + y z in deposited in the address of the e unit operation results. The concrete steps as follows:

(1) The input unit data switch place address as e;

(2) Opened the door of input three states, namely SW_G =0, LDAR =1 and negative pulse can be produced by press START switch T3 address e stored in registers;

(3)Input three states the door closed, namely SW_G =1,LDPC =0. Buy the S3 S0 M CN = 011000 S1 and S2 can get the result of x + y z in DATA BUS unit display;

(4) 299_g =0, by making the PC_G from 1 to 0 first and then to 1 will produce negative pulse data x + y z in the address for e storage unit, at the same time buy LDPC = 1.

Remove x + y z operation results and to display the OUTPUT unit. The concrete steps as follows:

(1) The input unit data switch place address as e;

(2) Opened the door of input three states, namely SW_G =0, LDAR =1 and negative pulse can be produced by press START switch T3 address e stored in registers;

(3) Input three states the door closed, namely SW_G =1, buy 299_g =0 in DATA BUS unit to read DATA x + y;

Complete the test process

Through the experiment of attachment and operation, on the one hand, students can connect each module, constitute a computer hardware system, on the other hand, through to the signal control operation, the control process of the controller and the working process of the arithmetic unit, thereby further form a concept of the machine in the link. In addition, the experiment used box as ZY15Comp12BB, if use other manufacturer experiment box, can be reference to complete the experiment design and operation, the study of the course so as to achieve purpose. All in all, the experiment in the teaching reform of computer constitute principle, has a certain reference value.

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