Voltage-Integration CMOS Image Sensor with Circuit-Sharing

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Abstract. An improved voltage-integration CMOS image sensor is presented. Some circuits is shared between the voltage integration block and the analog-to-digital convertor (ADC) through an optimal operation timing, which makes use of the different input-signals selected by the switches. Dynamic range expansion is realized, whereas the power consuming and the circuit area in the improved structure do not significantly increase because there is only one integrator and one subtracter. The proposed image sensor structure, designed on 0.18um CMOS process under 3.3V supply, verifies the feasibility of the design approach.

Introduction

During the past twenty years, a wide dynamic range (DR) CMOS image sensor is required for many applications such as scientific research, consumer application, and machine vision[1,2]. Many methods have been proposed to expand the dynamic range: (1) logarithmic or linear-logarithmic sensor[3-6], (2) well capacity adjusting[7-11], (3) multi-capture with different exposure time[12-14], (4) measurement of time to reach a threshold voltage by using a counter and a comparator placed in a pixel[12],[15], (5) self-resetting or charge subtraction to increase the effective well capacity[16-22]. Although the aforementioned CMOS image sensor designs provide a wide DR, these sensors have performance deficiencies such as the output limited by the finite well capacity, no CDS circuit to eliminate noise, low spatial resolution due to many frame memories and the adverse factors introduces by the comparator.

We proposed an idea to expand the dynamic range by using voltage-integration. The proposed structure is not limited to the potential well capacity, and switch linear response to nonlinear response automatically according to the illumination intensity without any decision circuit. Compared to the conventional structure, the fill factor and the power consuming are affected by the extra integration circuit. To mitigate the impact on these, the improved voltage-integration CMOS image sensor which shares some circuits between the voltage integrator and analog-to-digital convertor is proposed.

The paper is organized as follows. The principle of the voltage integration image sensor for dynamic range expansion is described in Section Ⅱ. The proposed circuit-shared image sensor is shown and detailed in Section Ⅲ. The simulation results are presented in Section Ⅳ, and conclusion is drawn in Section Ⅴ.

Principle of Dynamic Range Expansion

A common 3T-pixel image sensor which is composed of a photodiode (PD), a reset transistor (M1) and the source follower (M2, M3) is shown in Fig.1. In the conventional CMOS image sensor, the photon flux is converted into photocurrent i_{ph} by the PD. i_{ph} is a good measure of the incident photon flux since this process is linear. The resulting photocurrent is typically too small to measure directly, and thus it is integrated into the charge. After integration duration T_{int}, the charge is converted linearly to a voltage. The accumulated photo voltage V_{ph} is directly proportional to the photocurrent level, and can be expressed as

$$V_{ph} = \frac{i_{ph}T_{\text{int}}}{C_{\text{int}}} \qquad (1)$$

where i_{ph} is the photocurrent which is linear with the illumination intensity, T_{int} denotes the integration time, and C_{int} represents the integration capacitor.
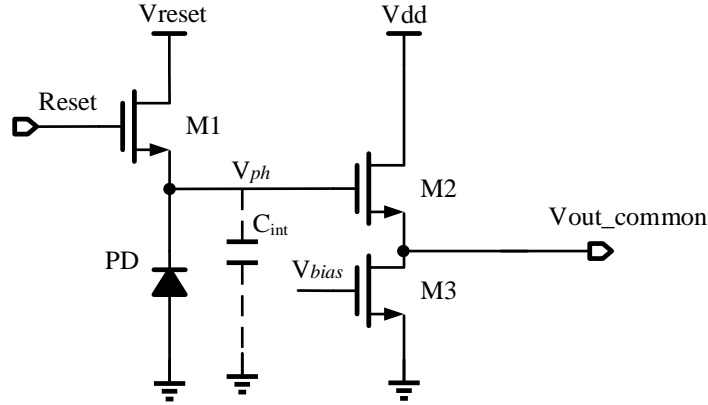

Fig. 1 Diagrams of the common 3T-pixel image sensor

The swing of V_{ph} is limited by the pixel circuit: the largest value is equal to the Vreset which is smaller than Vdd by a threshold value of M1 to realize the hard-reset mode in case of the lag and nonlinearity[23]; the smallest value is not less than $V_{od3}+V_{gs2}$ to ensure the source follower (SF) operate in the saturation region. So the range of V_{ph} is

$$V_{od3} + V_{gs2} \leqslant V_{ph} \leqslant Vdd - V_{th1} \tag{2}$$

where V_{th1} is the threshold value of the M1, V_{gs2} denotes the gate-source value of the M2, and V_{od3} represents the overdrive value of the M3. Thus, the range of the photocurrent i_{ph}, namely the dynamic range (DR), is limited by the finite voltage.

In order to expand the dynamic range in the finite voltage range, a voltage integration image sensor structure was proposed by using the integral area of the accumulated photo voltage within the T_{int} to characterize the photocurrent. The diagram is described in Fig.2.
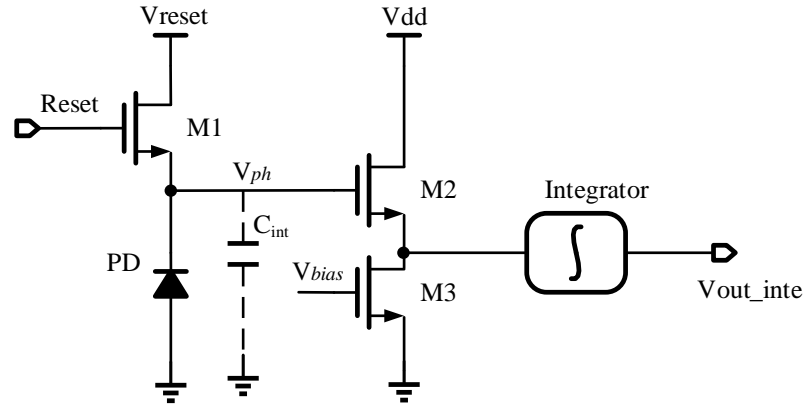

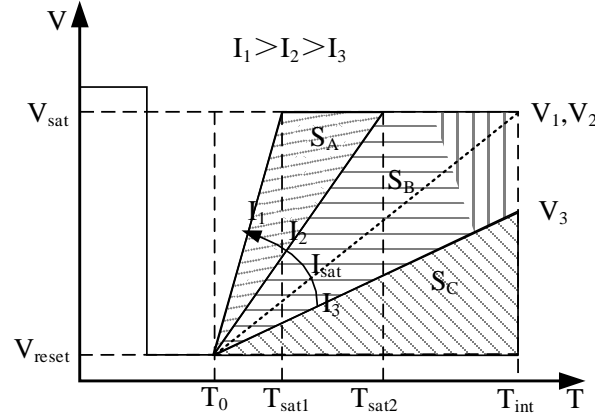Fig. 2 Diagrams of the voltage integration-type image sensor

Fig. 3 Outputs of the different photocurrents

To explain the principle of the proposed method, Fig.3 shows the outputs of the different photocurrents of the common output and the proposed integration output. S_A, S_B and S_C represent three dimensions with different shadow respectively. As shown in Fig.3, when the photocurrents, i.e., I_1 and I_2 exceed the saturation photocurrent i_{sat}, the integration areas $(S_A+S_B+S_C)$ and (S_B+S_C) are different since the time to saturation voltage T_{sat1} and T_{sat2} are different, even though the accumulated photo voltages $V1$ and $V2$ are the constant V_{sat}. Moreover, the proposed method characterizes the photocurrent in the expansion range by using the time to saturation without saturation-decision circuit which is applied in Ref.15. The output of the proposed method is given by

$$V_{out} = \begin{cases} \dfrac{1}{2}V_{ph}\left(T_{int}-T_0\right) & i_{ph} \leq i_{sat} \\ V_{sat}\left(T_{int}-T_0\right)-\dfrac{1}{2}V_{sat}\left(T_{sat}-T_0\right) & i_{ph} > i_{sat} \end{cases} \tag{3}$$

where T_0 is the starting time of integration, and the time to saturation T_{sat} is given by

$$T_{sat} = \frac{V_{sat}C_{int}}{i_{ph}}+T_0 \tag{4}$$

substituting (2), (4) into (3), one can obtain

$$V_{out} = \begin{cases} \dfrac{\left(T_{int}-T_0\right)^2}{2C_{int}}i_{ph} & i_{ph} \leq i_{sat} \\ V_{sat}\left(T_{int}-T_0\right)-\dfrac{V_{sat}{}^2C_{int}}{2}\cdot\dfrac{1}{i_{ph}} & i_{ph} > i_{sat} \end{cases} \tag{5}$$

From (5), the proposed method is composed of two responses in the wide illumination intensity range: one response is linear when i_{ph} is smaller than i_{sat}, otherwise the other response is nonlinear.

The structure diagram is shown in Fig. 4, where a single-port CDS circuit is introduced to reduce KTC and FPN noise. The output and sensitivity response are plotted in Fig.5. The output voltage is of the same order of magnitude. The simulation result shows that the dynamic range factor (DRF) is about 16dB, which verifies the proposed method. But the sensor area and power consuming are increased because of one more voltage integrator in the voltage integration image sensor compared to the tradition 3T CMOS image sensor.
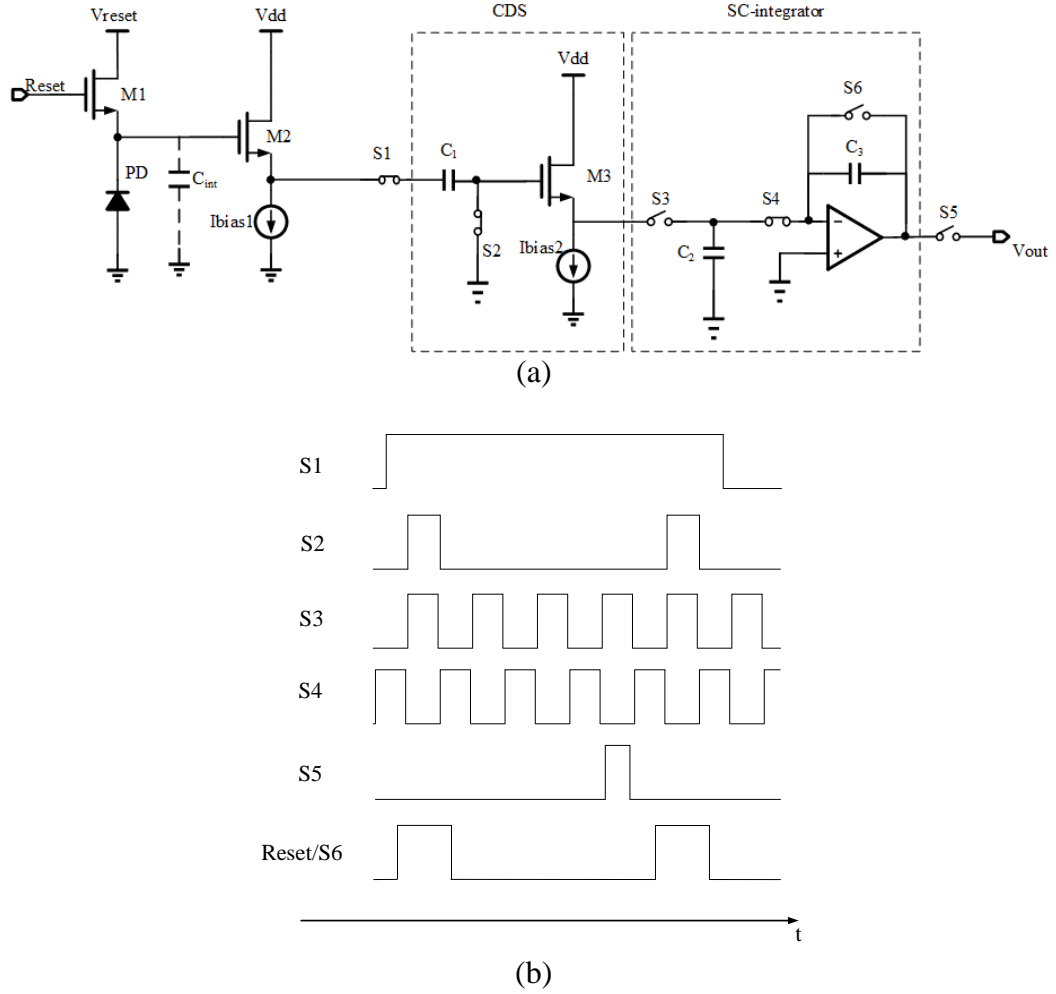
Fig. 4 The integration-type CMOS image sensor based on SC circuit
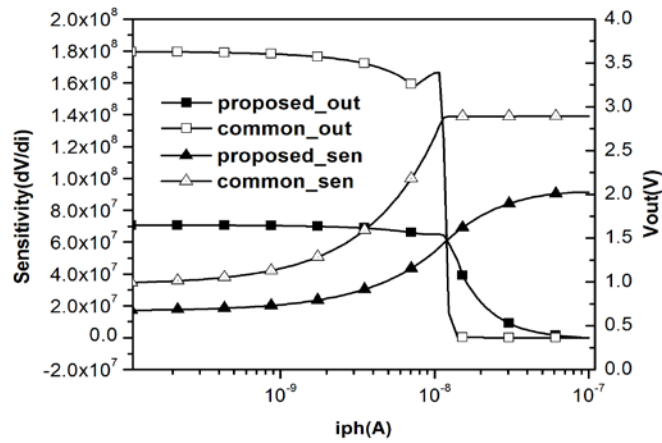(a) the diagram of the circuit, (b) the timing of the circuit

Fig. 5 Output responses of both the common and the proposed integration structures

Proposed Structure of the Circuit-sharing Image Sensor

ADC is an essential part because the analog readout signal has to be converted into digital for data processing. Incremental sigma-delta ADC structure is widely used in sensor applications with low frequency signal, which has the advantages of simple structure, low power consumption and loose demand of circuits and components. Fig.6 illustrates the block diagram of the incremental

sigma-delta ADC. The circuit is composed of a comparator for quantization, a DAC, an analog subtracter , an integrator and a counter used as a decimating filter[24].
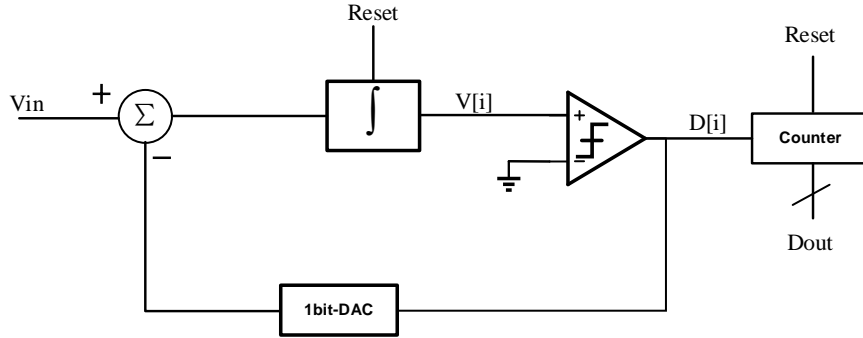

Fig. 6 Diagrams of the incremental sigma-delta ADC

As shown in Fig.4 and Fig.6, the subtraction and integration processes exist in both of the voltage integral pixel architecture and the sigma-delta ADC. Therefore, the two structures are merged by sharing the subtracter and integrator to mitigate the impact on the fill factor and power dissipation. The structure diagram is shown in Fig.7. The input of the subtracter is connected to the output of the pixel, the output of the integrator or the output of the 1-bit DAC, which is selected through the 3-1 Multiplexer. The optimal operation timing of switches, shown in Fig.7(b) are controlled by seven phases of the clock signal. In the clock phases, two non-overlapping clock phases control SW5 and SW6, which are shown as SW5/-SW6 for concise.
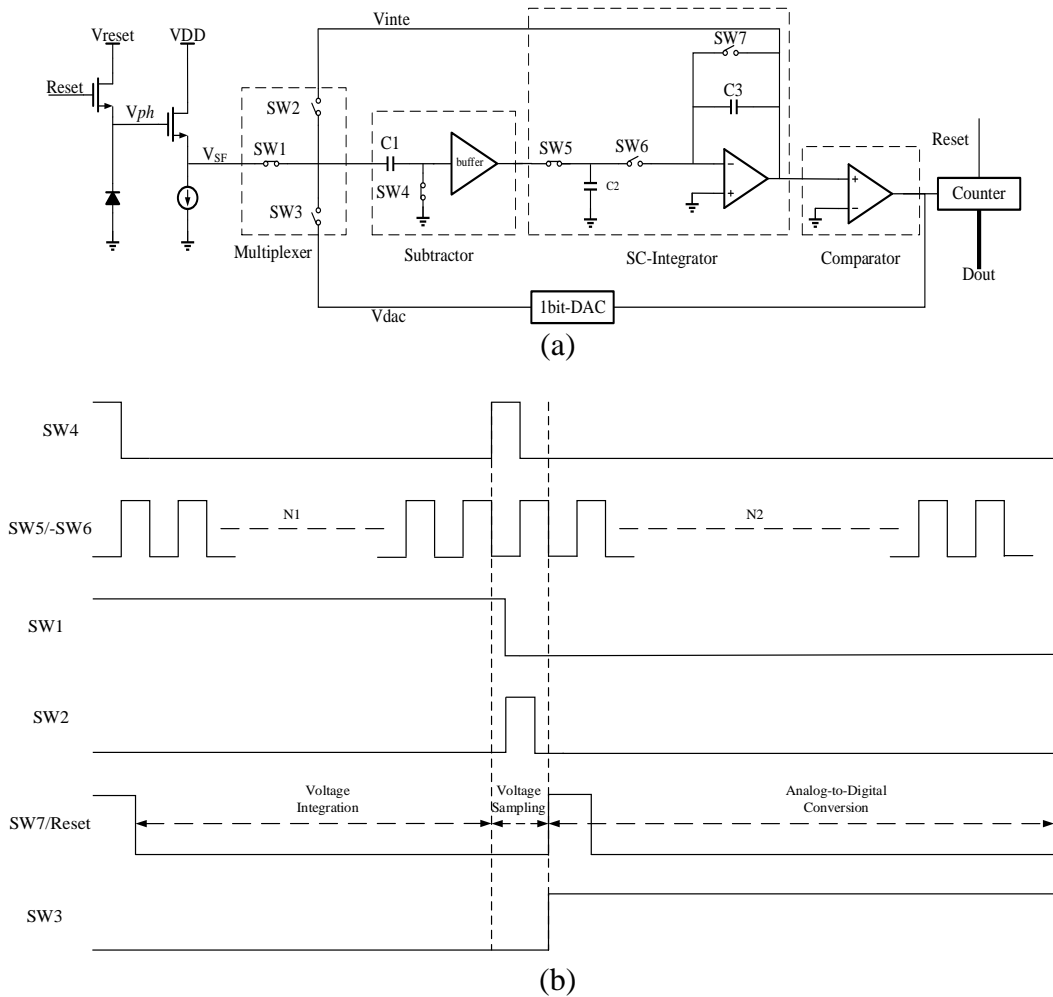

(a)

(b)

Fig. 7 The proposed circuit-sharing integration-type CMOS image sensor
(a) the diagram of the circuit, (b) the timing of the circuit

The circuit has three operating modes which is selected by the optimal operation timing to achieve the pixel-voltage integration and the analog-digital conversion with sharing the subtracter and the integrator. The three operating modes are described below with reference to Fig.7.

a) Integration Mode (I-MODE): Pixel-voltage integration mode for DR expansion is selected through SW1. During the reset period, SW4 is closed to obtain the reset voltage V_R of the pixel on C1. The amount of charge of C1 keeps constant while SW4 is opened. The right end voltage of C1 is (V_{SF}-V_R) after the reset, which realizes the true CDS. The non-overlapping clocks control SW5/SW6 to achieve the voltage integration. To prevent overload, the ratio of C3/C2 should be greater than or equal to the sampling number N1 in an exposure period.

b) Sampling Mode (S-MODE): After the I-MODE, open SW1 and close SW2/SW4 to sample the output voltage of the integrator. The voltage at the moment of SW4 opening is stored on C1 and SW2 is opened later for the next mode.

Conversion Mode (C-MODE): Reset the integrator and close the SW3 to form the incremental sigma-delta ADC which realizes the analog-digital conversion of the integrated voltage stored on C1, where N2 is the sampling number corresponding to conversion accuracy.

Simulation Results

To verify the feasibility of the design approach, the proposed image sensor structure is designed on 0.18μm CMOS process under 3.3V supply. Since the threshold value is about 0.8V and the overdrive value is about 0.3V, the maximum output-voltage of the SF is about Vdd-V_{th1}-V_{th2}-V_{od2}=1.4V. And thus the swing of the SF is 0V~1.4V. In order to observe whether the ADC works properly in this range, the input voltage is scanned from 0V to 1.5V. Fig.8. shows that the ADC has the ability to convert all the voltage in the range. Due to the offset of the signal path, the data obtained at 0V is 88 which is can be used in the subsequent digital CDS to eliminate the column FPN and offset. The entire structure is simulated to get the analog and digital outputs versus the photocurrent. The result of the integrated simulation is shown in Fig.9. The results validate the structure of dynamic range expansion while increasing the circuit area and power consuming very much. The simulation results also show nonlinearity caused by the body effect of the buffer between the subtracter and the integrator, which will be one of the future improvements.
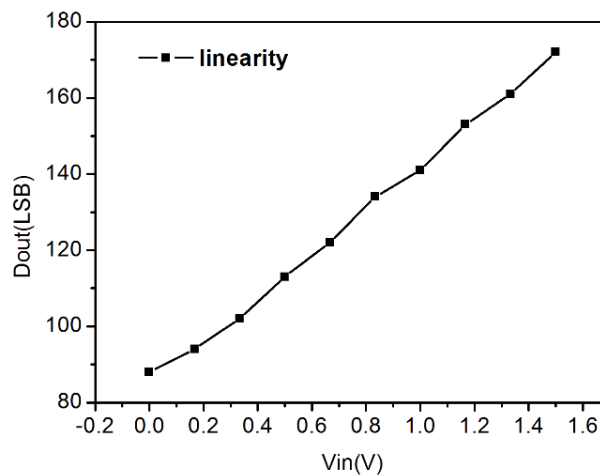

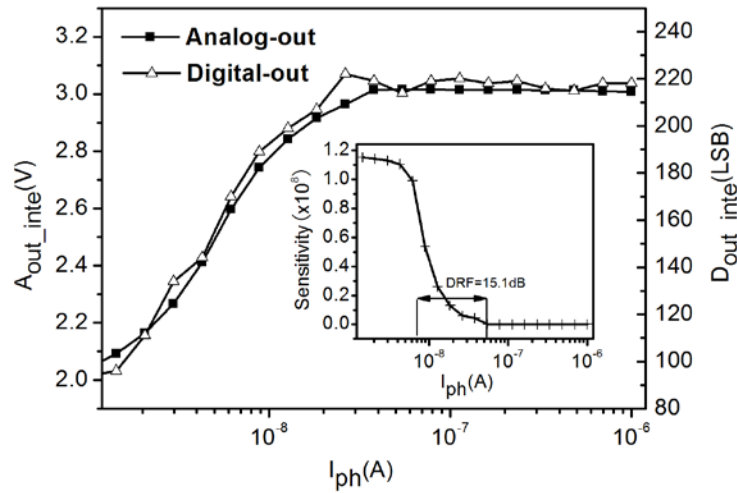Fig. 8 linearity of the incremental sigma-delta ADC

Fig. 9 Output responses of the proposed circuit-sharing integration-type image sensor structure

Summary

A circuit-sharing voltage-integration CMOS image sensor structure is proposed. As demonstrated in this paper, the proposed design approach has potential for the dynamic range expansion while not significantly increasing the circuit area and power consuming caused by the integrator. The main purpose of this paper is just to verify the feasibility of the design approach. The subsequent work will be the detailed analysis of the noise and the speed to optimize the performance of this method.

Acknowledgments

References

[1].   A. Darwish, G. Sicard, L. Fesquet, "Low data rate architecture for smart image sensor." *IS&T/SPIE Electronic Imaging. International Society for Optics and Photonics*, California, USA, pp. 902206-902206 (2014). [doi: 10.1117/12.2036851].

[2].   J. Yuan and H. Y. Chan, "Apparatus and method for improving dynamic range and linearity of CMOS image sensor." U.S. Patent No. 8,625,012. 7 Jan. (2014).

[3].   A. Spivak, A. Belenky, A. Fish, and O. Yadid-Pecht, "Wide-dynamic-range CMOS image sensors—comparative performance analysis." *Electron Devices, IEEE Transactions on*, **56**(11), pp. 2446–2461 (2009). [doi: 10.1109/TED.2009.2030599].

[4].   G. G. Storm, J. E. D. Hurwitz, D. Renshaw, et al, "High dynamic range CMOS image sensor using combined linear-logarithmic response from a CMOS image sensor," *IEEE Workshop on CCD and AIS* (2003).

[5].   B. Choubey and S. Collins, "Models for pixels with wide-dynamic-range combined linear and logarithmic response." *Sensors Journal, IEEE*, **7**(7), pp.1066–1072 (2007). [doi: 10.1109/JSEN.2007.895959].

[6].   S.H. Jo, M. Bae, P. Choi, and J.K. Shin, "Wide dynamic range CMOS active pixel sensor using a feedback structure." *Computer Science and Automation Engineering (CSAE), 2012 IEEE International Conference on*. **3**, pp. 363–366 (2012). [doi: 10.1109/CSAE.2012.6272973].

[7].   S. Decker, R. D. McGrath, K. Brehmer, et al, "A 256x256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output," *IEEE J. Of Solid-State Circuits*, **33**(12), pp. 2081–2091 (1998). [doi: 10.1109/ISSCC.1998.672423].

[8].   V. Berezin, I. Ovsiannikov, D. Jerdev, et al, "Dynamic range enlargement in CMOS imagers with buried photodiode." *IEEE Workshop on CCD and AIS* (2003).

[9].   A. El Gamal, "High dynamic range image sensors," *Tutorial at International Solid-State Circuits Conference*, **290** (2002).

[10].   S. Sugawa, N. Akahane, S. Adachi, et al, "A 100 dB dynamic range CMOS image sensor using a lateral overflow integration capacitor," *ISSCC***2005** ，Digest of Technical Papers, **19** (2005). [doi: 10.1109/ISSCC.2005.1494014].

[11].   W. Lee, N. Akahane, S. Adachi, et al, "A high S/N ratio and high full well capacity CMOS image sensor with active pixel readout feedback operation," *ISSCC***2007**, Asian, pp. 260-263 (2007). [doi: 10.1109/ASSCC.2007.4425780].

[12].   S. Kavusi and A. El Gamal, "Quantitative study of high-dynamic-range image sensor architectures," *Electronic Imaging* **2004**. *International Society for Optics and Photonics*, pp.264–275 (2004). [doi: 10.1117/12.544517].

[13].   D. X. Yang, A. E. Gamal, B. Fowler, et al, "A 640x512 CMOS image sensor with ultra wide dynamic range floating-point pixel-level ADC," *IEEE J. of Solid-State Circuits*, **34**(12), pp. 1821–1834 (1999). [doi: 10.1109/ISSCC.1999.759263].

[14].   T. Yamada, S. Kasuga, T. Murata, et al, "A 140dB-dynamic-range MOS image sensor with in-pixel multiple-exposure synthesis," *ISSCC***2008**. Digest of Technical Papers, pp.50–594 (2008).

[15].   D. Stoppa, A. Simoni, L. Gonzo, et al, "Novel CMOS image sensor with a 132-dB dynamic range," *IEEE J. of Solid-State Circuits*, **37**(12), pp.1846–1852 (2002). [doi: 10.1109/JSSC.2002.804347].

[16].   C. Jun, R. Feng, Y. Hui, X. Meihua, "A CMOS Image Sensor with Self-Reset Circuit in Active Pixel." *Image and Signal Processing***2009**, 2nd International Congress on. pp.1–4 (2009). [doi: 10.1109/CISP.2009.5301121].

[17].   D. Park, J. Rhee, Y. Joo, "Wide dynamic range and high SNR self-reset CMOS image sensor using a Schmitt trigger." *Sensors*, pp. 294–296 (2008). [doi: 10.1109/ICSENS.2008.4716439].

[18].   Z. Ignjatovic, D. Maricic, M. F. Bocko, "Low Power, High Dynamic Range CMOS Image Sensor Employing Pixel-Level Oversampling Analog-to-Digital Conversion." *Sensors Journal, IEEE*, **12**(4), pp. 737–746 (2012). [doi: 10.1109/JSEN.2011.2158818].

[19].   D. Maricic, Z. Ignjatovic, M. F. Bocko, "An oversampling digital pixel sensor with a charge transfer DAC employing parasitic capacitances," *MWSCAS'09*, pp.415–418 (2009). [doi: 10.1109/MWSCAS.2009.5236066].

[20].   D. Maricic, Z. Ignjatovic, D. F. Figer, et al, "Fully digital image sensor employing delta-sigma indirect feedback ADC with high-sensitivity to low-light illuminations for astronomical imaging applications," in *SPIE Astronomical Telescopes+ Instrumentation, International Society for Optics and Photonics*, 774217 (2010). [doi: 10.1117/12.857391].

[21].   Z. Gao, J. C. Liobe, M. F. Bocko, et al, "Indirect-Feedback Sigma-Delta Image Sensors: Theory, Modeling and Design," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, **61**(1), pp. 48–60 (2014). [doi: 10.1109/TCSI.2013.2268512].

[22].   J. Kim, W. Jung, S. Lim,et al, "A 14b extended counting ADC implemented in a 24Mpixel APS-C CMOS image sensor," *ISSCC***2012**, pp.390–392 (2012). [doi: 10.1109/ISSCC.2012.61770602].

[23].   I. Takayanagi, M. Shirakawa, K. Mitani, et al. "A 1.25-inch 60-frames/s 8.3-M-pixel digital-output CMOS image sensor." *Solid-State Circuits, IEEE Journal of*, **40**(11), pp. 2305-2314 (2005). [doi: 10.1109/JSSC.2005.857375].

[24].   J. Márkus, J. Silva, and G.C. Temes, "Theory and applications of incremental ΔΣ converters." *Circuits and Systems I: Regular Papers, IEEE Transactions on,* 51(4), pp. 678-690 (2004).

[25].   [doi: 10.1109/TCSI.2004.826202].