

A Wideband Low Noise Amplifier Based on Distributed LC Network

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Abstract. A CMOS wideband low noise amplifier (LNA) based on distributed LC network is presented in this paper. Employing the distributed LC network, the bandwidth of the low noise amplifier is greatly increased without sacrificing the gain of the amplifier. The amplifier is designed in 65nm CMOS process. Simulated result shows that the gain of the amplifier is 21.8 dB, while the 3dB bandwidth is 7.3 GHz from 21.5 GHz to 28.8 GHz. The input and output return loss are -13.6 dB and -16.5 dB at 24 GHz, respectively. The noise figure is 2.87 dB at 25.2 GHz and below 4 dB from 19.6 to 31.3 GHz. The amplifier consumes 14.9 mA current from 1.2 V voltage supply. The layout area of the amplifier is 0.66*0.48 mm² including all pads.

Introduction

Low Noise Amplifier (LNA) is one of the most important circuit modules in radio frequency (RF) receivers for communication and radar systems. Usually the LNA is placed at the first stage of the receiver which is used to amplify the weak signal received from the antenna. The signal is then processed by the following mixers or other circuit modules. The sensitivity of the receiver is dominated by the noise factor (NF) of the LNA. The noise of the following stages can be suppressed by the LNA.

The main performance specifications of LNA include NF, gain, bandwidth, input and output matching and linearity. During these specifications, bandwidth is one of the most important. For a radar system, the range resolution is usually inverse proportion to the bandwidth. Higher the bandwidth is, better the range resolution. For a wireless communication system, wider bandwidth means the achievable data rate is higher. The bandwidth of the receiver is affected by the bandwidth of LNA. Wide bandwidth LNA is required for high range resolution radar or high data rate wireless communication system. Transformer coupling and resistance feedback techniques have been proposed to increase the bandwidth of the LNA [1-2]. In this paper, a wideband LNA based on the distributed LC network is proposed. The bandwidth can be enlarged without sacrificing the gain of the LNA.

The paper is organized as follows. Section II describes the operation principle of distributed LC network and the implementation of the LNA. Section III gives out the simulated results of the proposed LNA. Conclusions are drawn in Section IV.

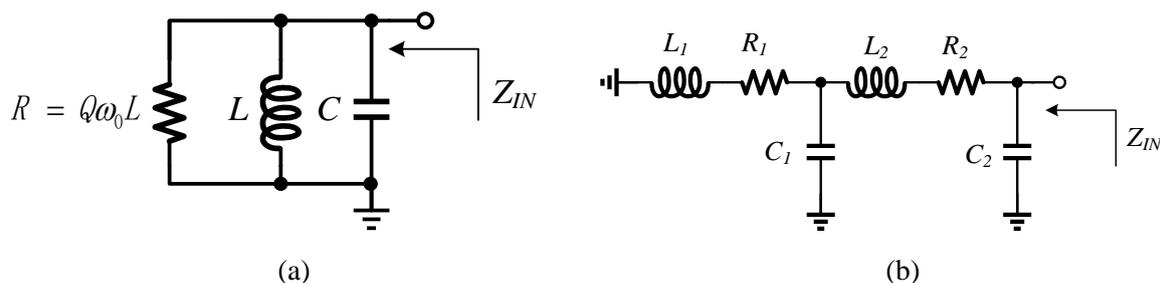


Fig. 1 (a) conventional LC network, (b) distributed LC network

Design and Analysis of LNA

Distributed LC network

In a conventional LNA in RF frequency range, inductors are usually used to resonator with the parasitic capacitance of the transistors in order to achieve a high gain at the operation frequency. The resonator can be simplified to the schematic in Fig. 1(a), in which L is the resonator inductor, C is the parasitic capacitor, and Q is the quality factor of the resonator. The 3 dB bandwidth and the peak of the input impedance of the resonator can be calculated as:

$$Z_{IN,MAX} = Q\omega_0 L$$

$$BW_{3dB} = \frac{\omega_0}{2\pi Q}$$

From these two equations, it can be seen that there is a tradeoff between the bandwidth and the gain. When the quality factor Q increases, the input impedance of the resonator increases, thus the gain of the amplifier increases. However, the bandwidth decreases when Q increases. It is not easy to achieve both wide bandwidth and high gain using conventional RLC resonator.

In this work, distributed LC network is used for inters-stage matching instead of the conventional RLC network, which can improve the bandwidth without sacrificing the gain of the amplifier compared with conventional RLC network. The distributed LC network has been used in millimeter wave injection-locked frequency dividers in [] to achieve high operation frequency. The schematic of the distributed LC network is shown in Fig. 1(b). To simplify the analysis, it is assumed that $L1=L2=L/2$, $C1=C2=C/2$.

Firstly we assume R in Fig. 1(b) is zero and consider a lossless distributed LC network. The input impedance can be calculated as:

$$Z_{in} = \frac{2s^3 L^2 C + 16sL}{s^4 L^2 C^2 + 12s^2 LC + 16}$$

The resonance frequency of the distributed LC network can be calculated by letting the dominator equals to zero:

$$s = j(\sqrt{5} \pm 1) / \sqrt{LC}$$

There are two resonance frequencies of the distributed LC network. Since the loss of the passive devices is usually higher at high frequency, the amplifier is chosen to work at the first resonance frequency of the distributed LC network.

The input impedance and bandwidth of the distributed LC network and the conventional RLC network is compared by simulation. To fairly compare the performance, it is assumed that the total capacitance of the two networks is the same. The resonance frequency and the peak impedance are the same by chosen proper inductance and Q, respectively. The simulated result is shown in Fig. 2.

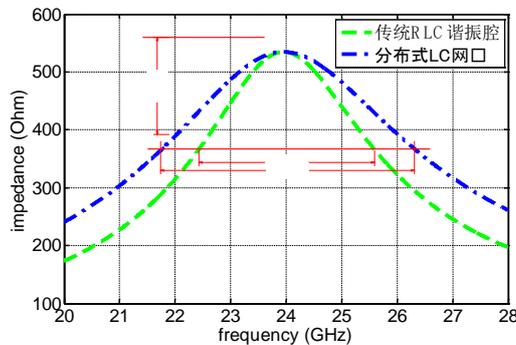


Fig. 2 simulated input impedance of the conventional RLC resonator and the distributed LC network

From Fig. 2, we can see that when the peak impedance and the resonance frequency are same, the 3 dB bandwidth of the distributed LC network is 1.43 times that of the conventional RLC network, which means the distributed LC network can improve the bandwidth of the amplifier

without sacrificing the gain.

Noise and input matching

The input terminal of the LNA should be noise matched and conjugate matched at the same time. In this design, it is realized using inductive source degeneration technique. The input impedance of the LNA after using the inductive source degeneration is:

$$Z_{IN} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s$$

In which, C_{gs} is the parasitic gate to source capacitance of the input transistor, L_g is the series connected inductor between input terminal and the gate of the input transistor and L_s is the source degeneration inductor. When the following equation is satisfied, the input terminal of the LNA is matched to 50 Ohm:

$$\omega(L_g + L_s) = \frac{1}{\omega C_{gs}}$$

$$\frac{g_m}{C_{gs}} L_s = 50\text{ohm}$$

The noise figure of the LNA is mainly dominated by the first stage. The noise contribution of the following stages is suppressed by the gain of the first stage. Thus the source degeneration inductor is eliminated in the second stage in order not to sacrifice the gain of the second stage. The chip area also benefits from the reduction of an inductor.

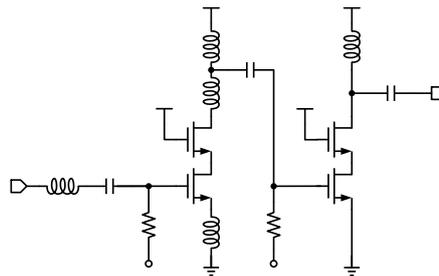


Fig. 3 the proposed LNA based on distributed LC network

Schematic of the LNA

The schematic of the proposed LNA is shown in Fig. 3. A two-stage cascode amplification structure is chosen for its high gain, good reverse isolation and stability. The first stage is composed with transistors M1A and M1B. L_s is the source degeneration inductor. As mentioned before, the input noise matching and power matching can be realized simultaneously using inductance source degeneration. L_g is used to tune out the negative image part of the input impedance. Transistors M2A and M2B are the second stage. The first and second stages are connected by distributed LC network composed of L_1 , L_2 and the parasitic capacitance of M1B and M2A to achieve wideband matching. The bias voltage is provided through bias network R_1 , C_1 , R_2 and C_2 . The decoupling capacitor of the supply voltage is not shown in Fig. 3.

The current density of the transistors in this design is chosen to be 0.15mA/um. As discussed in [4], the noise performance of the transistor is optimal on this condition.

Simulated Results

The proposed wideband LNA is designed in 65nm CMOS process, the layout of which is shown in Fig. 4. The area of the LNA including all the PADs is 0.66*0.48 mm². It consumes 14.9 mA current from 1.2 V supply voltage.

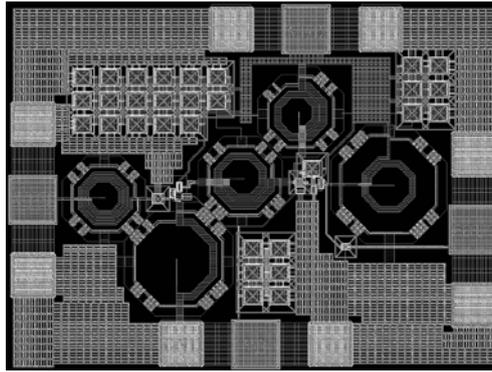


Fig. 4 The layout of the proposed LNA

Fig. 5 shows the simulated small signal performance. It can be seen that, the input return loss (S_{11}) and output return loss (S_{22}) at 24 GHz are -13.6 dB and -16.5 dB, respectively. The gain (S_{21}) at 24 GHz is 21.8 dB. Thanks to the distributed LC network, the 3-dB bandwidth is 7.3 GHz from 21.5 GHz to 28.8 GHz, which is about 30.4%. The simulated noise figure performance is shown in Fig. 6. The NF is only 2.87 dB at 25.2 GHz, and below 4 dB in the frequency range from 19.6 GHz to 31.3 GHz.

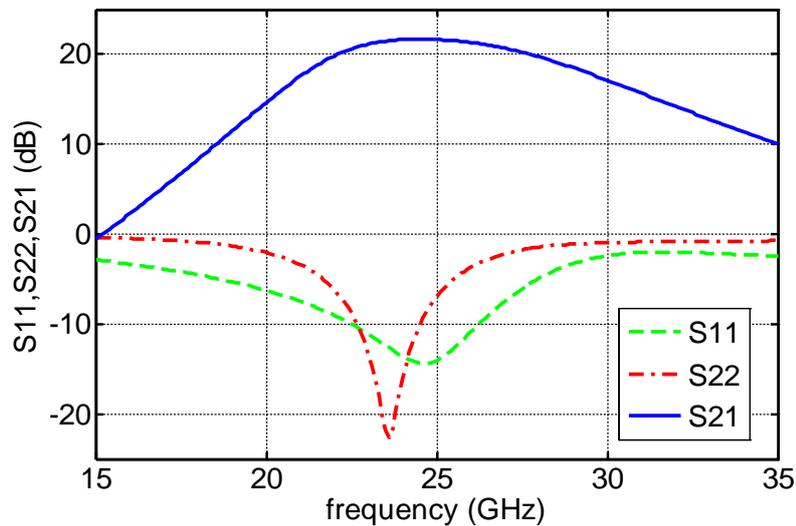


Fig. 5 The simulated S-parameters of the proposed LNA

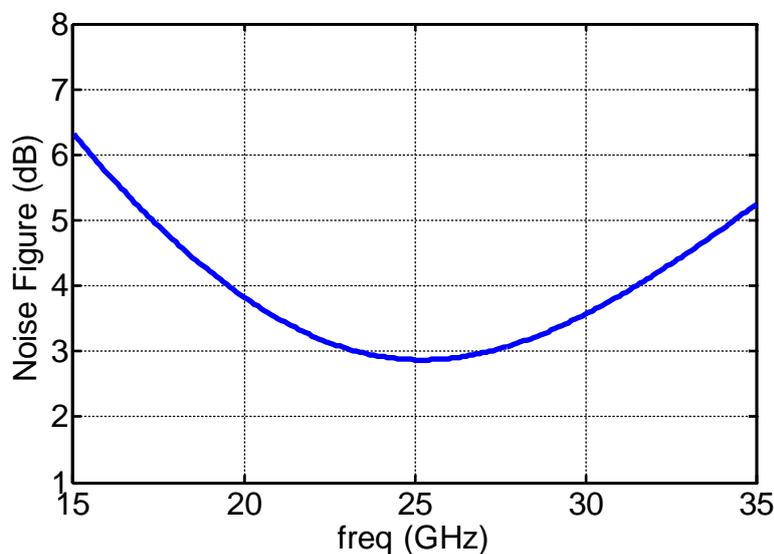


Fig. 6 The simulated noise figure of the proposed LNA

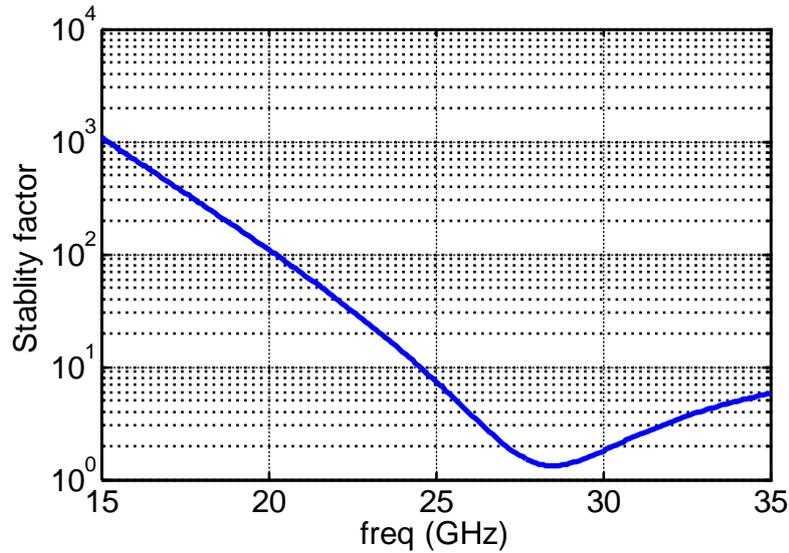


Fig. 7 The simulated stability factor of the proposed LNA

The stability is another critical parameter of LNAs. The stability can be measured using stability factor K , which is calculated from S-parameters [3]:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}$$

in which,

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

Fig. 7 shows the simulated stability factor of the LNA. The stability factor is greater than 1 from 15 GHz to 35 GHz, which means the LNA is unconditional stable in this frequency range.

Conclusions

In this paper, a wideband LNA based on distributed LC network is proposed. The distributed LC network is theoretically analyzed, which can increase the bandwidth without sacrificing the gain of the amplifier. The LNA is designed in 65nm CMOS process. Simulated results shows that the gain of the amplifier is 21.8 dB, the 3 dB bandwidth is 7.3 GHz from 21.5 GHz to 28.8 GHz. The noise figure at 25.2 GHz is 2.87 dB. The simulated results show the effectiveness of the distributed LC network.

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