The simulation and analysis of effect of vacuum eutectic welding parameters on void fraction of solder joint

Tiansheng Pang[1, a], Zhaohua Wu[2, b]

[1]School of Guilin University of electronic technology, Guilin 541004, China;

[2] School of Guilin University of electronic technology, Guilin 541004, China.

[a]547264458@qq.com, [b]1278396881@qq.com

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Abstract. The vacuum eutectic solder joint is widely used in the advantages of large thermal conductivity, small thermal resistance and so on. But the void ratio of vacuum eutectic solder has a great influence on the thermal conductivity, and the smaller the void ratio is, the greater the thermal conductivity coefficient is. Therefore, it is very necessary to optimize the parameters of vacuum eutectic welding process and reduce the void ratio of solder joints. In this paper, the three-dimensional finite element simulation model of the welding of the GaAs chip and the heat sink is established by using ANSYS software. The peak temperature, cooling rate and pressure as the main welding parameters of vacuum eutectic solder joint were selected as the main welding parameters[1]. In the method of keeping the two parameters unchanged for another parameter of the change, such as changing the cooling rate and the other parameters remain unchanged for simulation, similar to change pressure and peak temperature simulation and analysis of process parameters on the solder joint void rate effect rule, get the smallest solder joint void rate combination of process parameters. The research shows that the cooling rate has the most significant effect on the void of vacuum eutectic solder joint. In the range of 1.5℃/s ~2℃/s, with the increase of cooling rate, the void ratio increases, the maximum is 8.148% at 1.6℃/s, and then remains stable. The peak temperature is less important. On the simulation of the void rate of parabolic law, in the peak temperature range of 300℃~310℃, with the increase of the peak temperature, the simulation after the void first increases and then decreases, at 307℃ to 8.148%. The effect of pressure is the smallest, with the increase of pressure, the void ratio remains unchanged after simulation. According to the analysis of the process parameters of the simulation, the vacuum co crystal welding solder joint void rate minimum combination of process parameters: peak temperature is 307℃, the cooling rate is 1.5℃/s, the pressure is 400~2000Pa.

1. Introduction

With the rapid development of high power chip, the requirements for heat dissipation of the chip is higher, and the solder joint of vacuum eutectic solder has the advantages of large thermal conductivity, small thermal resistance and so on. The vacuum eutectic welding process parameters have significant influence on the void ratio of solder joints. For example, in the high power chip vacuum eutectic welding, cooling rate over the General Assembly increased solder joint void rate, chip welding surface hole will resulting in thermal contact resistance (coefficient of thermal conductivity of reciprocal) becomes large, so the heat generated by the chip cannot promptly sent out, which may cause device burnout failure. So it is important to study the influence of vacuum eutectic welding parameters on the void ratio of vacuum eutectic solder joint. The GJB548B-2005 in the clear provisions of the standard can not be received: welding contact area of the entire length of the hole than the length or width of the range, and more than the whole of the contact area of the 10%[2]. Based on the above reasons, application in high power chip vacuum eutectic welding need low solder joint void rate (less than 10%), then you need to vacuum eutectic bonding process parameters optimization in order to achieve 10% below the solder joint void rate, meet the cooling demand of high power chip.

2. The constitutive model of the vacuum eutectic solder

In this paper, the vacuum eutectic solder uses in Au80Sn20 (AuSn solder), the AuSn solder has the advantages of high thermal conductivity, high welding strength and without welding flux etc[3]. In the simulation software, the AuSn solder uses the generalized Anand constitutive model[4], and the model can explain the temperature dependence of the material, the rate dependence, the historical effect of strain rate, and the phenomenon of strain hardening. The basic form of using Anand to express the visco plastic property is:

The deformation resistance is proportional to the equivalent stress:

$$\sigma = cs\,, \qquad c < 1 \tag{1}$$

Among them, the c is a material parameter, and it is constant in the constant strain rate, which can be expressed as:

$$c = \frac{1}{\xi}\sinh^{-1}\left\{\left[\frac{\dot{\varepsilon}_p}{A}\exp\left(\frac{Q}{RT}\right)\right]^m\right\} \tag{2}$$

In formula (2): $\dot{\varepsilon}_p$ is a non elastic strain rate, A is constant, Q is the activation energy; m is the strain rate sensitive index; ξ is the stress multiplier; R is the gas constant; T is the temperature.

The evolution equation can be expressed as:

$$\dot{s} = h(\sigma, s, T)\dot{\varepsilon}_p - \dot{\gamma}(s, T) \tag{3}$$

The formula (3) is related to the dynamic strain hardening and recovery, which can be expressed as:

$$h(\sigma, s, T) = \left[h_0\left|1 - \frac{s}{s^*}\right|^a sign\left(1 - \frac{s}{s^*}\right)\right] \tag{4}$$

and

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_p}{A}\exp\left(\frac{Q}{RT}\right)\right]^n \tag{5}$$

A is the deformation hardening softening constant, a is the strain sensitive index of the hardening softening, s^* is the internal variable saturation value, $\hat{s}$ is the coefficient, n is the index.

At the given temperature and strain rate, when the plastic deformation rate is consistent with the loading strain rate, the deformation of the material reaches the state of plastic flow, the stress reaches the saturated stress σ^*; Under the given temperature and stress conditions, the plastic flow of the material reaches the steady state when the saturated stress reaches the load. The deformation resistance of this material reaches the saturation point of s^*:

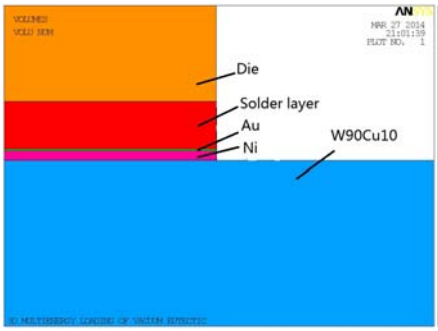
$$\sigma^* = cs^* \tag{6}$$

$$\sigma = \sigma^* - \left\{\left(\sigma^* - cs_0\right)^{(1-a)} + (a-1)\left[(ch_0)(\sigma^*)^{-a}\right]\varepsilon_p\right\}^{1/(1-a)} \tag{7}$$

3. The simulation model

This paper adopts heat sink W90Cu10 (tungsten copper alloy) as middle layer between substrate and the chip, from top to bottom: chip, solder layer (using schistose solder), gold plating, nickel plating, heat sink tungsten copper alloy (W90Cu10), the thickness of the chip is 0.1mm, the length

and width are 2mm×1mm. The length and width of the solder film, the gold plating layer and the nickel plating layer are the same, the thickness of the solder film is 0.025mm, the thickness of the nickel plating layer is 0.005mm, the thickness of the tungsten copper alloy is 0.2mm, the length is 3mm×1.1mm. In this paper, we mainly study the cavity between the chip and solder paste, solder paste and heat sink, so the substrate is simplified, and the geometrical model is shown in Figure 1. The whole model is divided into direct coupling of thermal structure with the SOLID5 unit and SOLID98 unit. The finite element mesh is shown in Figure 2.



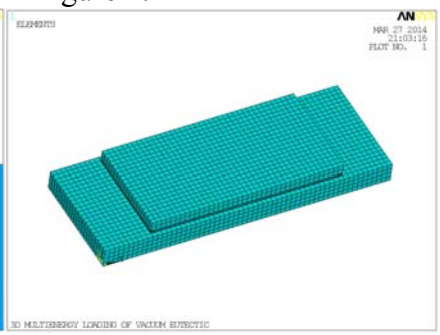


Figure 1 The vertical section of model Figure 2 The grid division of geometric model

According to the vacuum eutectic welding process, the pressure is made on the surface of a chip by a weight block or a tungsten needle. In the simulation software, the pressure is switched to intensity of pressure bear on the surface of the model, and the pressure is present in the whole welding process, so the pressure is constant and intensity of pressure of the surface is uniform. Taking into account the actual welding of the chip in the vacuum furnace welding is on the hot plate, so in the simulation temperature load is applied on the surface of the heat sink. The boundary conditions are fixed displacement constraints for the model of X, Y, and Z three directions on the bottom surface of the heat sink. There are preseting a certain number of voids in the solder layer before simulation (void ratio is 8.128%), because the simulation software is difficult to generate voids. In this paper, the solder joint void ratio of vacuum eutectic solder is controlled within 10%, and the voids will become larger and larger, so the hole rate of the preset should be less than 10%, as shown in Figure 3. The preset holes is cylindrical. According to the experimental results[6], it is easy to be found some large voids in the edge of the solder layer, so the paper presets some large holes in the edge of the solder layer.

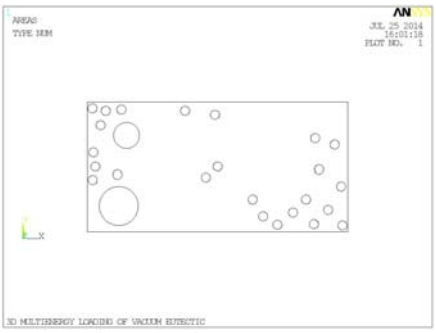


Fig. 3 The transverse section of the solder layer

After the simulation the voids are irregular, the cross-sectional area is not able to be extracted. If the hole is preset to a rectangular or cylinder, the thickness is in a certain range (less than 25 m), then the void ratio is approximately equal to the value of the void volume dividing the volume of the solder layer:

$$S^{'} \approx (V_1 - V_2)/V_1 \tag{8}$$

In formula (8), V_1 represents the volume of solder paste, and two quantities are agreed in this study: The solder layer effective volume (V_2) and approximate void fraction ($S^{'}$ refers to void ratio). The difference between V_2 and V_1 is the size of the solder layer. The effective volume of the solder layer is the area which can realize the function of the solder layer, such as heat conduction, electric conduction, sealing, etc.

4. The Simulation Analysis

4.1 The typical vacuum eutectic welding process

Three main technological parameters, i.e., the peak temperature, the cooling rate and the pressure, are considered in the vacuum eutectic solder joint voids. In this paper, the parameters of the typical vacuum eutectic welding process have an effect on the solder holes. The parameter combination of the typical vacuum eutectic welding process: the peak temperature is 305℃, the cooling rate is 1.75℃/s, the surface pressure is 1200Pa. The simulation results are shown in Figure 4, and the displacement of the chip is the largest and the displacement of the heat sink is the smallest.

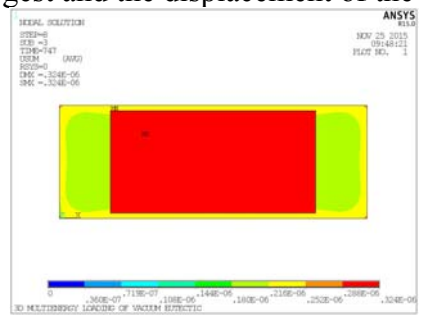


Fig. 4 The global displacement distribution of the model

4.2 The effect of welding process parameters on solder joint voids

In this paper, in order to test the parameters of each process, the 3 process parameters are set up according to the vacuum eutectic welding process parameters of chapter 3.1, and the two parameters are fixed to change the other parameters, and the 3 process parameters are changed in turn. The change rule of void ratio of the solder layer is analyzed, and then the process parameter combination of the minimum solder joint void ratio is obtained. 300℃, 303℃, 305℃, 307℃ and 310℃ of the peak temperature are taken, 1.5℃/s, 1.6℃/s, 1.75℃/s, 1.8℃/s and 2.0℃/ of the cooling rate are taken, 400Pa, 800Pa, 1200Pa, 1600Pa and 2000Pa of the pressure are taken. The void ratio of each process parameter was obtained, and the results are shown in Figure 5.

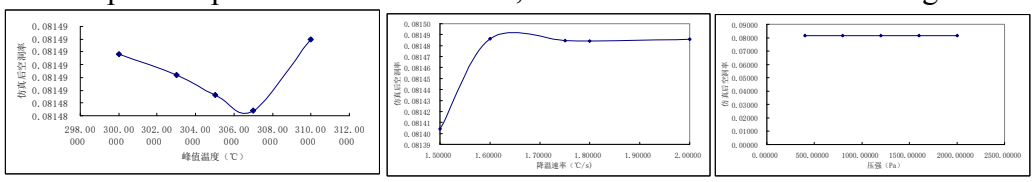


Fig. 5 simulation test of peak temperature, cooling rate and pressure

From Figure 5, the results show that the void ratio of solder joint decreases with the increase of the peak temperature firstly, and then increases. At 306℃ to 307℃, a certain value of this interval, the simulation of the void rate is minimum, at the minimum value of both sides of the peak temperature of the void will become large, in the subsequent peak temperature parameters can be considered to be about 307℃. With the increase of cooling rate, the void ratio also increases with the increase of temperature. When the cooling rate increases to 1.6℃/s, the rate of time and space is no longer changing, and tends to be stable. From Figure 5 that the void rate remains constant with the change of pressure, pressure in the simulation effects on the rate of hole is very small. Because the model of maximum stress is 0.367×e9Pa, maximum pressure and should force contrast is too small, almost no effect on the cavity change.

5. The vacuum eutectic welding parameters optimization

To sum up, we can know that the cooling rate is the main factor to affect the rate of cavity during the welding process, the peak temperature is the second, and the influence of the pressure is the least. So vacuum eutectic welding can choose moderate peak temperature and lower cooling rate, the peak temperature is 307℃, the cooling rate is 1.5℃/s. Due to the pressure in the simulation of solder joint void rate almost no effect, so the pressure of the preferred 400Pa~2000Pa, simulation of the solder joint void ratio of 8.140%, to achieve the minimum solder joint void ratio.

6. Summary

In this paper, ANSYS software is used to simulate and analyze the effect of welding process parameters on the void of solder joint. The study shows that the cooling rate is the main factor of void formation. With the increase of cooling rate, the rate of voids increases continuously, and the cooling rate increases to a stable level of 8.148% after the simulation of /s at 1.6℃/s. The peak temperature is the less important factor of cavity formation, and the void ratio increases with the increase of the peak temperature in the range of 300℃ to 310℃ after the first decreases to 8.148% and then increases to 8.149%. The pressure in the simulation of the formation of the void is not significant, empty rate remains unchanged. According to the simulation analysis, the optimum process parameters of vacuum eutectic solder joint void fraction (8.140%) are obtained: The peak temperature is 307℃, the cooling rate is 1.5℃/s, the pressure is 400~2000Pa, which provides a reference for reducing the void ratio.

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