Tracking technology on phase of PN code in spread spectrum communication

Wang Shaoshuai, Zhu Zebo, Fu Gang

China Satellite Maritime Tracking and Control Department, Jiangyin, 214431, China

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Abstract. Pseudo code phase tracking spread spectrum signal, we studied DLL, pseudo code discriminator algorithms are analyzed, with an emphasis on pseudo-code tracking loop performance analysis and simulation, obtained a series of valuable conclusions , has very important significance for the loop bandwidth settings.

1. Introduction

In a spread spectrum measurement and control system, one of the key issues is to extract the demodulated signal speed and distance information, so in order to ensure the receiver to work properly, variable parameter uncertainty when the code phase (ie, code delay) the receiving end it is necessary to grasp exactly. This chapter locked loop performance impact of latency by loop noise analysis, to design a suitable stable under high dynamic tracking loop bandwidth.

2. Delay locked loop (DLL)

Delay locked loop mainly by the relevant accumulator, a discriminator, a loop filter and a code NCO components. Figure 1 Block diagram of a non-coherent delay locked loop.

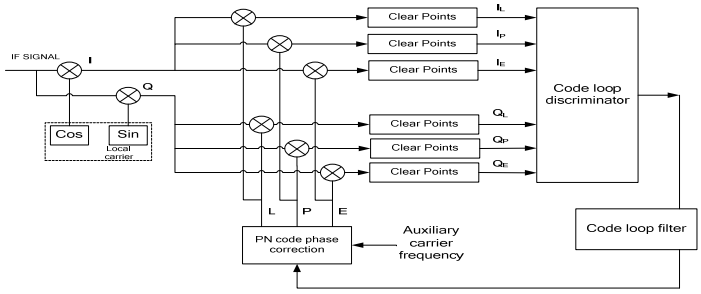


Figure 1. Full time lead - lag non-coherent delay locked loop block diagram

Delay-locked code tracking loop phase generally composed of both lead and lag associated receiving branch and a subtraction branch composed of lead, lag results after subtracting the relevant branch of the correction signal is formed, after the loop filter controls the amount of output error the control phase of the local code, so that the pseudo-code phase adjustment accordingly.

Delay-locked code tracking loop phase spreading sequence based on the principle of self-dual symmetry of the correlation function implementation.

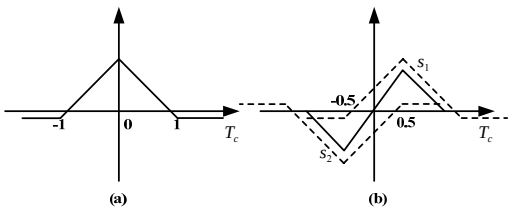


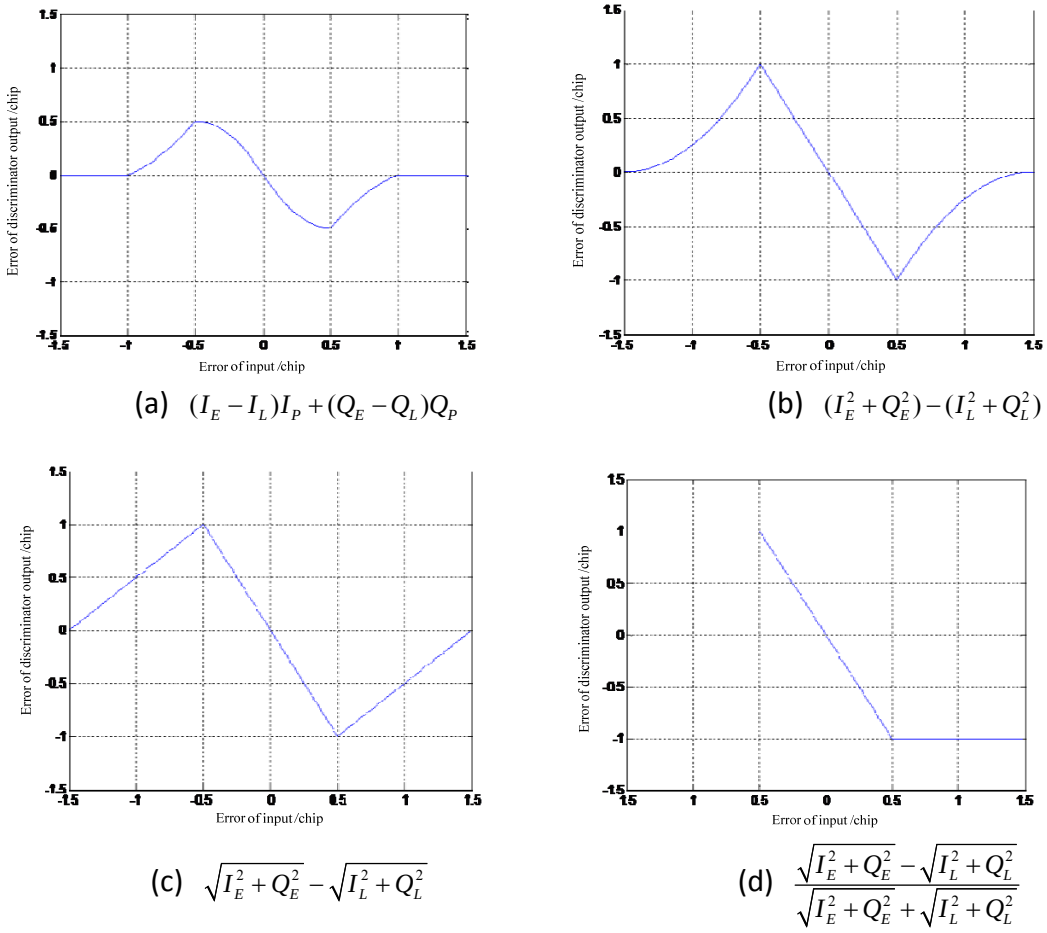
Figure 2. Using the delay, the autocorrelation curve ahead synthesis phase curve

Figure 2(a) is a pseudo code autocorrelation function, when $\tau = 0$, the maximum correlation value. Figure 2(b) since the broken line S_1 is shifted correlation function the autocorrelation function, i.e., the curve ahead of the relevant branch, the dashed line S_2 is the autocorrelation function of the autocorrelation function shifted, i.e., the hysteresis curve associated branches. Two

shift autocorrelation function subtraction, spreading sequence obtained tracking phase curve, namely FIG. 2(b) of the solid line. As can be seen, when the phase difference between the received sequence and zero sequence local, phase detector output is zero; when the phase difference is not equal to zero, then the phase detector outputs a proportional signal polarity, to control the phase of the local sequence to reduce the phase difference, closed-loop control.

3. Pseudo code discriminator algorithm analysis

Delay locked loop discriminator algorithm commonly used four. Dynamic performance and noise performance of the code tracking loop is conflicting, in order to reduce the noise measurement errors, generally desirable to use as small an interval associated with the noise bandwidth; and to the receiver has a strong ability to adapt to the dynamic nature of the carrier, then I hope the relevant interval and noise bandwidth can be as large as possible. For no auxiliary code tracking loop, in order to ensure discriminator linear operating range of the relevant interval you can not get too small, usually select the relevant interval of one-half chip, second-order or third-order loop filter, noise bandwidth determined according to the dynamic range.



(a) $(I_E - I_L)I_P + (Q_E - Q_L)Q_P$

(b) $(I_E^2 + Q_E^2) - (I_L^2 + Q_L^2)$

(c) $\sqrt{I_E^2 + Q_E^2} - \sqrt{I_L^2 + Q_L^2}$

(d) $\dfrac{\sqrt{I_E^2 + Q_E^2} - \sqrt{I_L^2 + Q_L^2}}{\sqrt{I_E^2 + Q_E^2} + \sqrt{I_L^2 + Q_L^2}}$

Figure 3. Compare delay locked loop discriminator algorithm

Figure 3 the four curves of the discriminator output of the algorithm were compared. The diagram assumes correlator spacing 1/2 chip, with the ideal and no noise associated trigonometric functions I, Q measurements. The reality is that due to the limited bandwidth of the receiver front end, on each side of the peak is not ideal linear ramp-up or ramp-down; the presence of noise makes the slope flattens and causes the slope discriminator edge becomes smooth.

Normalized advance minus-late discriminator envelope removed because of the sensitivity of the magnitude and has been widely used, but the dot product discriminator phase power and better performance of the minimum amount of computation, however, the dot product discriminator required advance , current and hysteresis three complex correlators signal improved method is to

first lead-minus-late local code together as a local composite signal, then the correlation operation, the advantage of doing so is to produce the desired lead minus the hysteresis signal only needs to be a complex correlators.

4. Measurement Error Analysis and Simulation

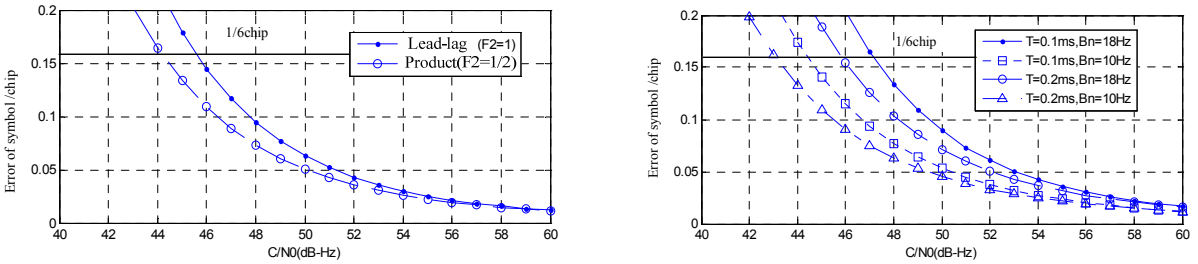
In pseudo-code tracking loop, a pseudo code phase estimation error source is the main error of the thermal noise dither and dynamic stress error. DLL experience tracking threshold value method is caused by the loop trembling all sources of stress, it is not allowed to exceed the number of chips correlator represented interval. Thus, tracking threshold of thumb is:

$$3\sigma_{DLL} = 3\sigma_{tDLL} + \sigma_{eDLL} \le d(\text{chip}) \quad (1)$$

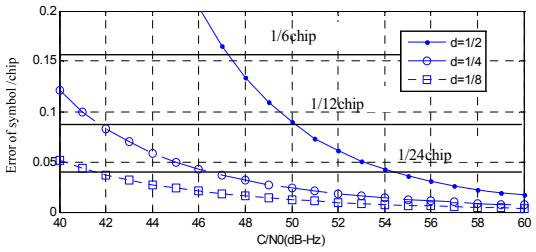
DLL code tracking fibrillation thermal noise is:

$$\sigma_{tDLL} = \sqrt{\frac{4F_1 d^2 B_n}{C/N_0}[2(1-d) + \frac{4F_2 d}{T \cdot C/N_0}]}(chip) \quad (2)$$

By the formula indicates, DLL fibrillation filter noise bandwidth proportional to the square root of that reduce the bandwidth to make quiver smaller, resulting in lower SNR threshold. At the same time, the cumulative increase integration time results in lower SNR threshold, but the degree of influence without reducing the bandwidth so much. In addition, the thermal noise has nothing to do with the order of the loop.



(a) Lead - lagging behind and product discriminator (b) Effect of integration time and noise bandwidth DLL jitter



(c)Jitter on DLL correlator spacing

Figure 4. Delay locked loop thermal noise performance under different circumstances

Figure 4 (a) the product and lead-lag DLL discriminator thermal noise performance were compared, where, $F_1 = 1/2$, $d = 1/2$, $B_n = 18\text{Hz}$, $T = 0.1\text{ms}$. As can be seen, on the threshold of about 1dB better product discriminator; Fig. 4 (b) reduce the noise bandwidth and simulated preflight reduced integration time to improve the situation DLL tracking threshold, wherein, $F_1 = 1/2$, $F_2 = 1/2$, $d = 1/2$; Fig. 4 (c) Comparison different performance-related DLL interval, wherein, $F_1 = 1/2$, $F_2 = 1/2$, $B_n = 10\text{Hz}$. It is worth noting that, while reducing associated interval, thermal noise is reduced, the threshold is improved, but the dynamic stress tolerance also declined.

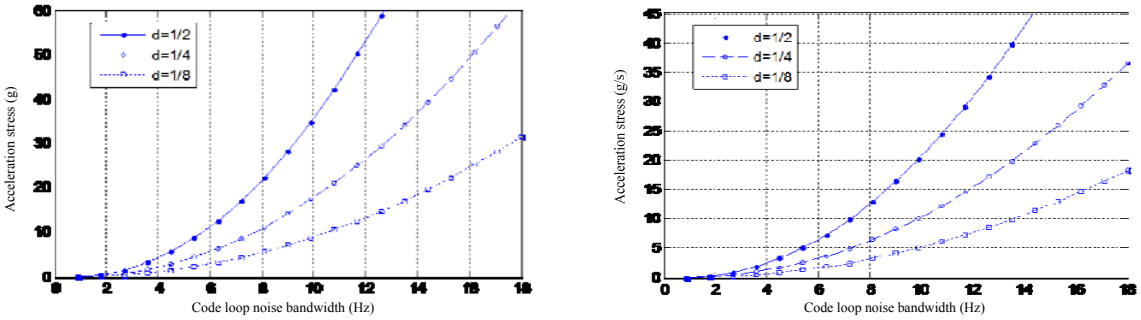
Dynamic stress error DLL tracking loop is determined by the following formula:

Second order loop:

$$\sigma_{eDLL} = \frac{dR^2/dt^2}{\omega_0^2} = \frac{d^2R/dt^2}{(B_n/0.53)^2} = 0.2809\frac{d^2R/dt^2}{B_n^2}(\text{chip}) \quad (3)$$

Third-order loop:

$$\sigma_{eDLL} = \frac{dR^3/dt^3}{\omega_0^3} = \frac{d^3R/dt^3}{(B_n/0.7845)^3} = 0.4828\frac{d^3R/dt^3}{B_n^3}(\text{chip}) \quad (4)$$



(a) Second Order DLL acceleration stress threshold (b) Third Order DLL jerk stress threshold

Figure 5. Dynamic Stress door code loop limit

Figure 5 (a) and 5 (b) describe the second-order and third-order DLL DLL is as a function of the noise bandwidth limit at d = (1/2) (1/4) (1/8) chip gate the dynamic stress. Wherein, Rb = 10.23Mchip / s, F1 = 1/2, preflight integration time 0.1ms, SNR = 50dB-Hz, it can be seen, the interval associated with the decrease, the dynamic performance of the code ring is reduced. Considering, for measurement and control code tracking accuracy of less than 3ns, code ring equivalent bandwidth to 10Hz, correlation intervals to take 1 / 4chip.

5. Summary

This paper code tracking loop measurement error analysis, the following conclusions can be obtained: the longer the integration time loop, code phase measurements in the thermal noise smaller; reduce the correlation interval and noise bandwidth, noise reduction loop heat, but dynamic tracking range will be smaller loop, the loop subjected to dynamic stress diminished capacity; code loop should be designed considering the integration time, interval and associated noise bandwidth settings.

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