

A Current-Compensation System for DC Offset in Transmitting Digital-Analogue Converter

DONG Hai^{1,a}, WANG Zong-min, KONG Ying

¹Beijing Microelectronics Technology Institute, Beijing, China

^ahitdonghai@163.com

Keywords: Auxiliary DAC, dc offset, compensation current

Abstract. This paper proposes a current compensation system for dc offset in transmitting digital-analogue converter (auxiliary DAC) firstly, which solves the DC offset existing in DAC output current. It greatly enhances the flexibility of the output DC offset controlling and improves the consistency of output currents between the chips. The auxiliary DAC proposed by this paper can compensate the DC offset ranging from -2mA to 2mA with the regulation accuracy at 1.96 μ A, which achieves a high accuracy of output the compensation current.

Introduction

The stability of transmitting DAC output current used in wireless communication devices military equipment and radar is essential [1]. Traditional DAC output current is generally fixed at 20mA, but it will make the output current dc offset due to the production process and the working environment [2]. As a result of it, the dc offset compensation current needs to be set depending on the different applications.

In a typical transmitting DAC, the dc offset compensation current is set by an external operational amplifier [3]. Different resistances are set to determine the different output currents depending on the applications. In the application of the transmitting DAC, external resistors are once set, the compensation current can't be changed. In practice, due to fluctuations of the process and working environment, dc offset in transmitting DAC is different, which requires the compensation current flexible depending on the application environment, but general transmitting DAC can't meet this requirement[4]. As a result, the dc offset compensation current is directly related to the accuracy of an external resistor in general transmitting DAC. Since the precision of resistors is limited and uncontrollable in board-level applications, the accuracy of the dc offset compensation current is also limited and uncontrollable [5]. In the applications requiring precise control, the general transmitting DAC can't meet the accuracy requirement.

Structure and principle of auxiliary DAC

A current compensation system for dc offset in transmitting digital-analogue converter named auxiliary DAC is shown in Fig. 1: including the bias circuit, the current source coarse tuning circuit, the current source fine-tune circuit and the current sink circuit. The specific method is as follows:

Bias circuit provides bias voltages, and the current sink circuit extracts from the current output terminal of the transmitting DAC. The current source coarse tuning circuit generates 32 the same currents, and the sum of the currents is equal to the current extracted by the current sink circuit. According to coarse tuning control signal, the top N channels current outputs are selected to the current output terminal, and the N + 1-th current output to the current source fine-tune circuit. The current source fine-tune circuit divides the N + 1-th current into 6 parts (1:1:2:4:8:16), and the fine-tune control signal select corresponding current output to the current output terminal. The present invention provides a flexible compensation current system for dc offset in transmitting DAC, increasing the accuracy of the output current and realizing precision control.

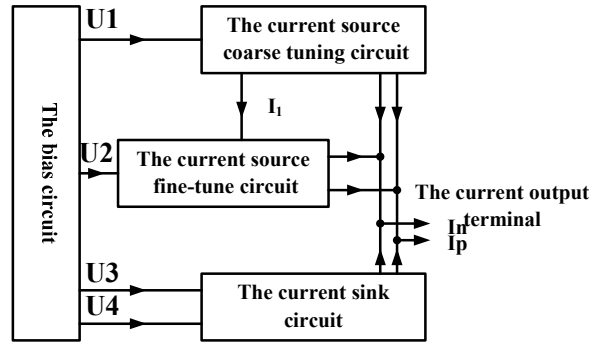


Figure 1 The current compensation system

Design of circuit structure

Specifically, the bias circuit supplies a bias voltage $U1$ for the current source coarse tuning circuit, and provides a bias voltage $U2$ to the current source fine-tune circuit and provides two bias voltages $U3$, $U4$ to the current sink circuit. Under the action of bias voltage $U3$, $U4$, according to the control signal input by the user, the current sink circuit extracts $I0$ from the current output terminal, which is the maximum current. The current source coarse tuning circuit under the action of the bias voltage $U1$ generates 32 the same currents $I1$; receiving five binary coarse tuning control signals, it selects the top N channel currents and outputs to the current output terminal. The $N+1$ -th current outputs to the current source fine-tune circuit. The $N+2$ -th current to 32-th current are connected with ground, in which $I1=I0/32$. N is the largest integer value to meet the $N \times I1 \leq I$ and $N \leq 31$. I is the expected compensation current. The current source fine-tune circuit receives the $N+1$ -th channel current from the current source coarse tuning circuit. Under the bias voltage $U2$, the current source fine-tune circuit divides it into 6 currents at the ratio of 1: 1: 2: 4: 8: 16, where in the first current is connected directly with ground. Receiving five binary fine-tune control signal input by the user, the current source fine-tune circuit selects corresponding current to the current output terminal, in which $I0-I-N \times I1-I2 < I0/(32 \times 32)$, and $I2$ is the current that the current source fine-tune circuit offers to the current output terminal.

Design of the current source coarse tuning circuit

As shown in Fig. 2 is the current source coarse tuning circuit which includes a thermometer decoder circuit, 32 groups of the same structure thermometer code current sources and 32 sets of the same structural thermometer code current source switches. The thermometer decoder decodes 5-bit binary coarse tuning control signals into 31 thermometer codes exporting them and 31 complement thermometer codes; a thermometer code current source and a thermometer code current source switch are connected to form a single current path (the current source of the switching control circuit). Each current source of switching control circuit provides enable port $EN1$, current flows selection port SE and sign port $SIGN$. When the enable port signal $EN1$ is 1, the current source of switching control circuit is working properly. When the enable port signal $EN1$ is 0, the current source of switching control circuit closes, and current flows to the ground. When the current flows selection port signal SE is 1, the current source of switching control circuit compensates the output current to the current output terminal. When the current flows selection port signal SE is 0, the current source of switching control circuit outputs current to the current source fine-tune circuit. When the sign port signal $SIGN$ is 1, the current source of switching control circuit compensates the output current to P current output terminal. When the sign port signal $SIGN$ is 0, the current source of switching control circuit compensates the output current to N current output terminal.

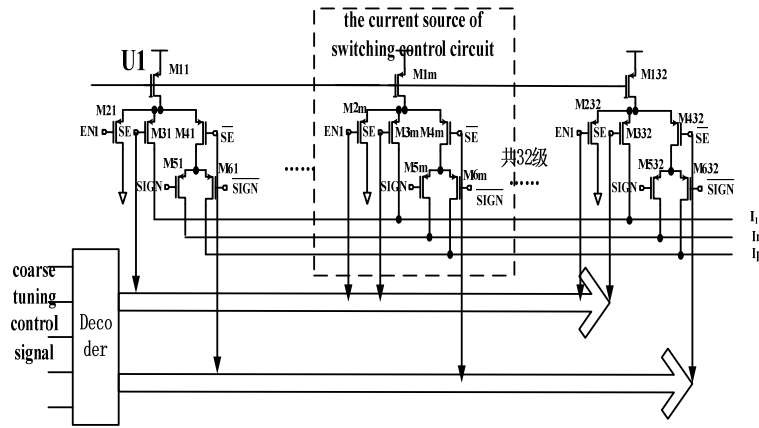


Figure 2 The current source coarse tuning circuit

By the decoder circuit 31 thermometer codes are used to control the port SE in the group 1th to group 31th of the current source selection of switch control circuit, and connect with the port EN1 in group 2th to group 32th of the current source of switching control circuit. The port EN1 in group 1th of the current source of switching control circuit is set to 1, and the port SE in group 32th of the current source of switching control circuit is set to 0. All 32 sign port SIGNs of the current source switches are parallel.

Design of the current source fine-tune circuit

Fig. 3 shows the current source fine-tune circuit structure in auxiliary DAC, comprising a carry current source, 5 groups of binary code current sources and 5 sets of the same structural binary code current source switches. The proportion of binary current in the current source is 1: 2: 4: 8:16. Each binary code current source switch provides enable port EN2 and sign port SIGN. When the enable port signal EN2 is 1, the binary code current source switch is working properly. When the enable port signal EN2 is 0, the binary code current source switch closes, and current flows to the ground. When the sign port signal SIGN is 1, the current compensates the output current to P current output terminal. When the sign port signal SIGN is 0, the current compensates the output current to N current output terminal. The current source fine-tune circuit receives 5 binary fine-tune control signals, which control the enable port EN2 of current source switch, determining current source circuit output compensation current. All 5 sign port SIGNs of the current source switches are parallel. Final accuracy of compensated output current for dc offset is within ± 1 LSB.

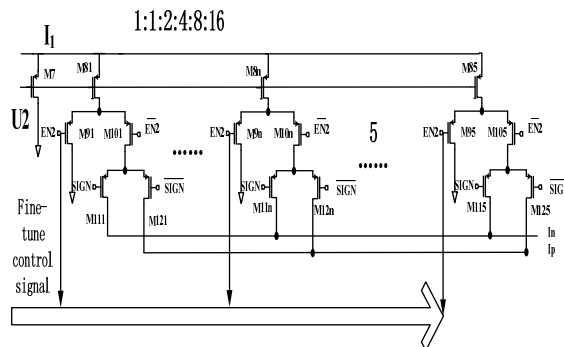


Figure 3 The current source fine-tune circuit structure

Design of the current sink circuit

Fig. 4 shows the current sink circuit in auxiliary DAC, which includes an encoder circuit, the switching circuit and the current sink circuit. Under the bias voltage U_3 , U_4 provided by the bias circuit, the current sink current extracts I_0 from the current output terminal. Encoder circuit receives external direction signal DIRECTION and sign signal SIGN, and encodes them into the control signal of switch circuit as follows $A = \text{DIRECTION} \& \text{SIGN}$, and $\bar{A} = \overline{\text{DIRECTION}} + \overline{\text{SIGN}}$,

and $B = \text{DIRECTION} \& \overline{\text{SIGN}}$, and $\overline{B} = \overline{\text{DIRECTION}} + \text{SIGN}$. Switch circuit controls current sink circuit. Wherein, when the DIRECTION signal is 0, the current sink circuit closes; when the DIRECTION signal is 1, the current extracts I_0 from the current output terminal. When the SIGN signal is 1, the current extracts I_0 from the P current output terminal; when the SIGN signal is 0, the current extracts I_0 from the N current output terminal.

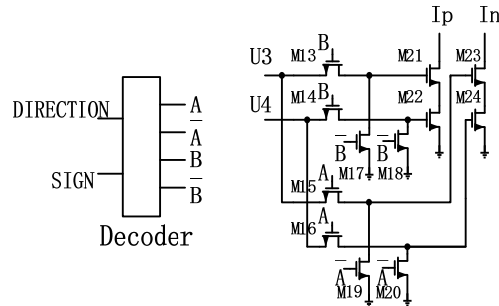


Figure 4 The current sink circuit

Results

Overall circuit diagram of the auxiliary DAC in this paper design is shown in Fig. 5:

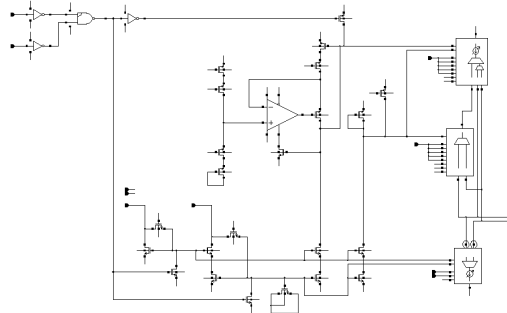


Figure 5 Overall circuit diagram of the auxiliary DAC

Fig. 6 shows the auxiliary DAC pours into the current ranging from 0 to 2mA. When the current sink circuit extracts 2mA current, auxiliary DAC extracts current ranging from 0 to -2mA. Therefore, the compensation current adjustment range of auxiliary DAC is -2mA to 2mA.

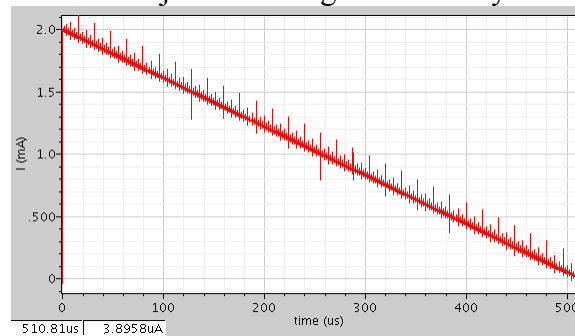


Figure 6 The current range of auxiliary DAC

Fig 7 shows that the output accuracy of auxiliary DAC compensation current is 1.93μA.

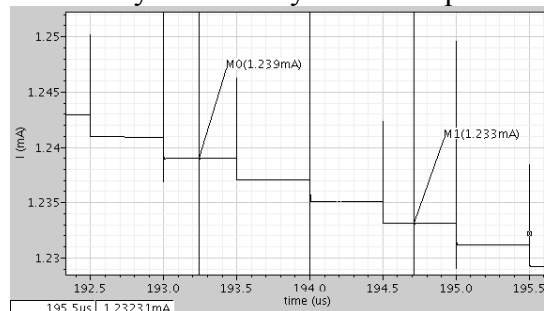


Figure 7 The output accuracy of auxiliary DAC

Summary

This project overcomes the deficiencies of the prior art and to provide a current compensation system for dc offset in transmitting DAC. It should solve imprecise adjustment problem in the dc offset compensation current, and how to solve the problem through the digital control, which improves the flexibility of DAC output current.

References

- [1] Gielen G. Systematic design of data converters. Circuits and Systems, 2001. Tutorial Guide: ISCAS 2001. The IEEE International Symposium on, 2001:6.3.1-6.3.14.
- [2] Jacob Winker. Studies on CMOS Digital-to-Analog Converters. Ph.D. thesis, Linkoping University, 2001.
- [3] Da-Huei Lee, Tai-Haur Kuo, Kow-Liang Wen. Low-Cost 14-bit Current-Steering DAC with a Randomized Thermometer-Coding Method. IEEE Transactions on Circuits and Systems. 2009, 2, 56(2). 137-141.
- [4] T. Miki et al. An 80 MHz 8 bit CMOS D/A converter. IEEE J. Solid-state Circuits. 1986, 21 (6):983-988.
- [5] Chi-Hung Lin, Klaas Bult. A 10-b, 500-MS/s CMOS DAC in 0.6mm². I IEEE J. Solid-state Circuits., 1998, 33(12).1948-1958.