

## Low Power Design of Shift Registers for Silicon Micro Display

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**Abstract.** A low design of condition-triggering shift registers on Silicon for display was proposed, which has a new circuit structure of input driver clock. The design only allows certain clocks to enter the register, so that the dynamic power has been reduced. It has been demonstrated that the proposed structure could ensure the signal to transport correctly while the power of the circuit to reduce effectively at the same time. As for the 320 bits register, the power could be reduced by the rate of 24.41%.

### 1. Introduction

With the rapid development of technology for LCoS and OLEDs, the micro-display chips on Silicon have become a hot research topic in the world. The micro-display system on Silicon with portable structures is charged by the battery, so the power consumption has become the critical factor of its promotion and development. In Reference<sup>[1~3]</sup>, the driver voltage varies at the same time as the display color. In Reference<sup>[4,5]</sup>, the circuit structure has been optimized. According to the working principle<sup>[6]</sup> of the micro-display chip, the scan driving circuit works in the highest frequency and consumes the most power in all the display circuits. The invalid flips of the clock into the shift registers bring excess dynamic power. In this paper, a new condition-triggering structure of the shift register is proposed to avoid excess the invalid clock flips effectively, resulting in reducing the dynamic power by controlling the clock into the shift register unit. The simulation results demonstrate that the power consumption of the shift registers with the newly-proposed D flip-flops has reduced to a great extent.

### 2. Dynamic Power Analysis of Micro-display Scanning Circuits

The line driver and the column driver in the micro-display chips on Silicon are integrated in the display chips. Either the line scanning circuit or the column scanning circuit contains high-speed SIPO shift registers. Besides the shift registers are formed by multi-bit series D flip-flops. The fig.1 shows the equivalent CMOS capacitance mode of the D flip-flops. When the voltage of the transmission gate's input port  $V_{in}$  changes, the voltage of its output port  $V_{out}$  changes. The dynamic power of the transmission has a relationship with parasitical capacitors, namely  $C_{gb1}$ 、 $C_{gb2}$ 、 $C_{gs1}$ 、 $C_{gs2}$ , and the load capacitor  $C_L$ . When  $V_{in}$  remains unchangeable,  $V_{out}$  won't change at all. In this situation,  $C_{gb1}$  and  $C_{gb2}$  won't charge or discharge at all. However, if bidirectional clock signals change,  $C_{gs1}$  and  $C_{gs2}$  connection to M1 and M2 will charge or discharge. That is to say, even if the input signal remains unchanged, the clock signals will lead to the dynamic power consumption of the transmission gates. Above all, in a row pixel scanning period, only two clock flips are invalid for each

flip-flop of the scanning shift registers column and the others are excess. The dynamic power could be calculated as equation (1).

$$P = C V_{dd}^2 f \quad (1)$$

In the equation, P is dynamic power and C is capacitor,  $V_{dd}$  is supply voltage and f is the frequency of the charging and discharging.

If the supply voltage remains stable, the excess dynamic power is proportional to the parasitical capacitors and the frequency of M1 and M2. The higher the display resolution is, the higher the clock's frequency is, thus the more the dynamic power is. In the 1918 clock cycles, the dynamic power consumption generated by the clock's flips is invalid during a row scanning for a 1920x1080 display screen.

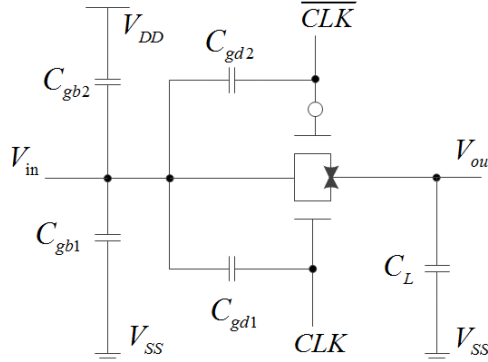


Fig.1 CMOS transmission gate capacitance model

### 3. Condition-triggering Shift Register's Unit Circuit

The principle of the newly-proposed shift register's unit circuit is shown as Fig.2. The inputs of the NOR gate G1 are connected to the input and the output of the D flip-flop and its output decides that whether the clock signal could enter the flip-flop's input. It is seen that only if both the flip-flop's D input's voltage and Q output's voltage are high, the clock signal could be allowed into the flip-flop's clock port. When the D input's voltage is high, a clock's positive edge could make the Q output's voltage high and when the next positive edge comes, the Q output's voltage turns to low. During the process, a pixel is selected successfully. Then after that, the clock port of the flip-flop will be shut up, thus the clock's invalid flips of the unit circuit are avoided during the period when the flip-flop isn't selected.

The unit circuit proposed this paper works only if both the D input's voltage and the Q output's voltage are high. In other situations, the circuit stands by. In summary, the dynamic power has been reduced effectively.

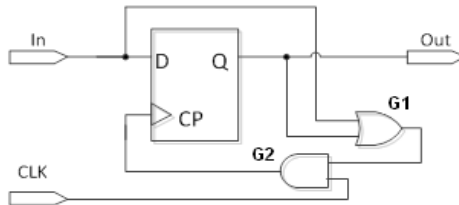


Fig.2 Condition-triggering shift register circuits

## 4. Layout and Functional Verification

### 4.1 Design of Layout

The circuit in this paper is designed by standard 180nm CMOS technology and a 640x480 resolution low power LCoS layout design has been completed with newly proposed condition-triggering shift registers. The column driver circuits distribute in the upper and lower sides of the display chip in a party way. Fig.3 shows 40-bit shift registers' layout, which is 1/8 part of odd column driver circuit including condition-triggering shift registers. The clock signal

transmits from left to right and the circuits in the red box control the clocks connecting to the condition-triggering registers. The control circuit of each register can be realized by only 8 MOSFET after optimizing the circuit shown in Fig.2. The area of the LCoS micro-display chip designed is 11mmx7.5mm and the layout's length of each flip-flop is 6mm in the column driver direction considering the chips cutting and the liquid crystal packaging, etc. Fig.3 shows that layout's width of the shift registers with condition-triggering flip-flops is 33.9um larger than the traditional shift registers in the column driver direction. Considering the upper and lower column driver circuits, the width in the column driver direction could be thought to add by 0.9%, that is to say the width of the complete chip increase 67.8um comparing to the earlier width of 7.5um with the same pixel pitch of 5.65um.

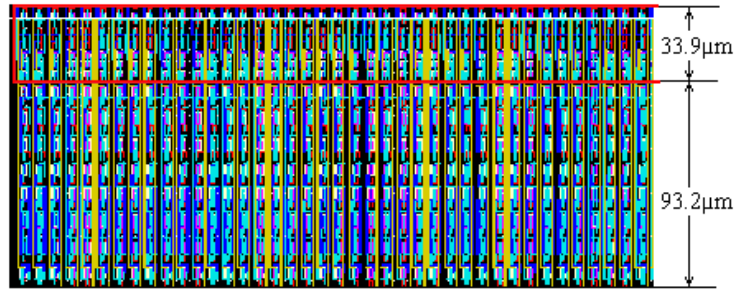
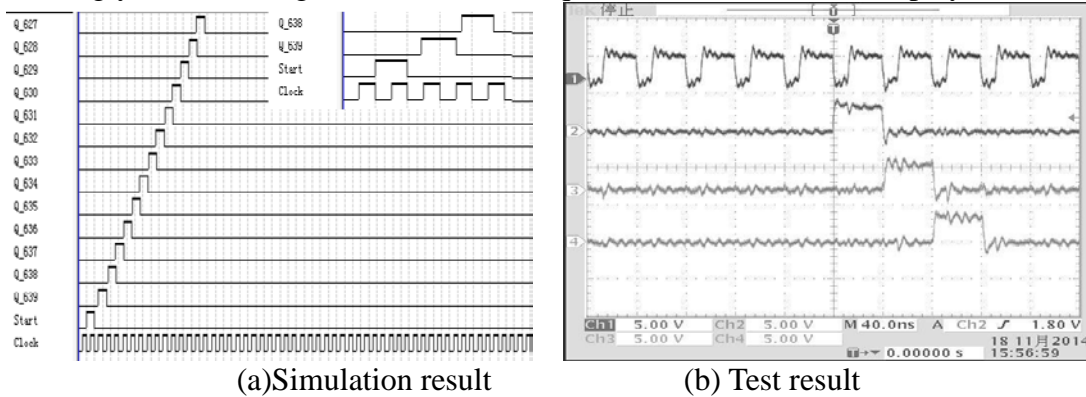


Fig.3 Layout of 40-bit condition-trigger shift registers unit circuit

#### 4.2 Functional Simulation and Verification

In order to verify the function of the newly designed condition-triggering shift register, a circuit model of 640-bits condition triggering shift registers is built in QUARTUS and simulated. The wave of shift registers' output signals Q0, Q1, ..., Q639 is given by Fig.4(a). From Fig.4 (a), it is demonstrated that the high levels of the data strobe signals are transferred in turn successfully, meeting the needs of the scanning signals of the on Silicon micro-display chips.

The 640-bits condition-triggering shift registers are verified in the FPGA hardware of the chip EP1K30TC144 belonged to Altera. Depending on the requirement of the circuits of VGA resolution display, the clock's frequency of the condition-triggering shift registers is 30MHz. After testing any 3 continuous output signals of the registers in Tektronix TDS3054 digital storage oscilloscope, it could be proved that the test results, shown in Fig.4 (b), are consistent with the simulation results. It confirms strongly that the design meets the time requirements of the micro-display on Silicon.



(a)Simulation result

(b) Test result

Fig.4 Result of the condition-triggering shift registers

#### 5. Power verification

In order to verify the power consumption of the condition-triggering shift registers, Design Compiler from Synopsys is used to simulation the registers with new flip-flops and the traditional structures. In order to compare the power, this paper assumes P as the dynamic power of the N-bits traditional shift registers, P1 the condition-triggering and the relative dynamic power reduction rate A could be expressed as equation (2).

$$A = \frac{P - P1}{P} \quad (2)$$

From the analysis above, it is clear that the bigger the bit N is, the more relative dynamic power reduction A is. In this paper N is selected as 10, 40, 80, 120, 160, 200, 240, 280 and 320. The final simulation data of relative power reduction is shown in table 1.

Table 1 Relative power reduction rate of N-bits registers

N	10	40	80	120	160	200	240	280	320
P(uW)	120.08	467.60	956.91	1425.0	1893.0	2363.4	2843.5	3309.8	3774
P1(uW)	109.83	415.03	812.69	1192.7	1556.7	1904.8	2237.1	2552.8	2852.6
A(%)	9.33	11.24	15.07	16.3	17.77	19.4	21.33	22.87	24.41

In this paper, Matlab is used to fit the approximate relationship between A and N, finding an approximate equation shown as (3).

$$A=0.05298N+11.15 \quad (3)$$

From the formulation (3), A is 36.58 when N =480. Meanwhile, the result of A from the simulation of Design Compiler is 39.17 while the N equals the same value of 480. The error between the results obtained in two different ways is 7.08%. Thus the fitting formulation (3) can be regard reasonable. The simulation results show that the shift registers proposed in this paper could minify the power by 24.41% for odd column driving circuits (N =320).

## 6. Conclusions

A research on low power design of the micro-display on Silicon has been presented and a condition-triggering shift registers has been proposed in this paper. For each unit circuits, only if the voltage levels of both the data input and output are high, it will work. Otherwise it will remain in a state of standby, leading to a signification dynamic power reduction resulting from the invalid flips. With the timing simulation and the hardware verification in FPGA, it is demonstrated that the shift registers proposed in this paper work in right timing sequence and satisfy the requirement of the scanning circuit of the micro-display chip on Silicon. Both the simulation from Design Compiler and the theory analysis from Matlab prove that the dynamic power has been reduced by a large degree and the power of the 320-bits condition-triggering shift registers has decreased by 24.41 contrasting with the traditional circuits.

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